

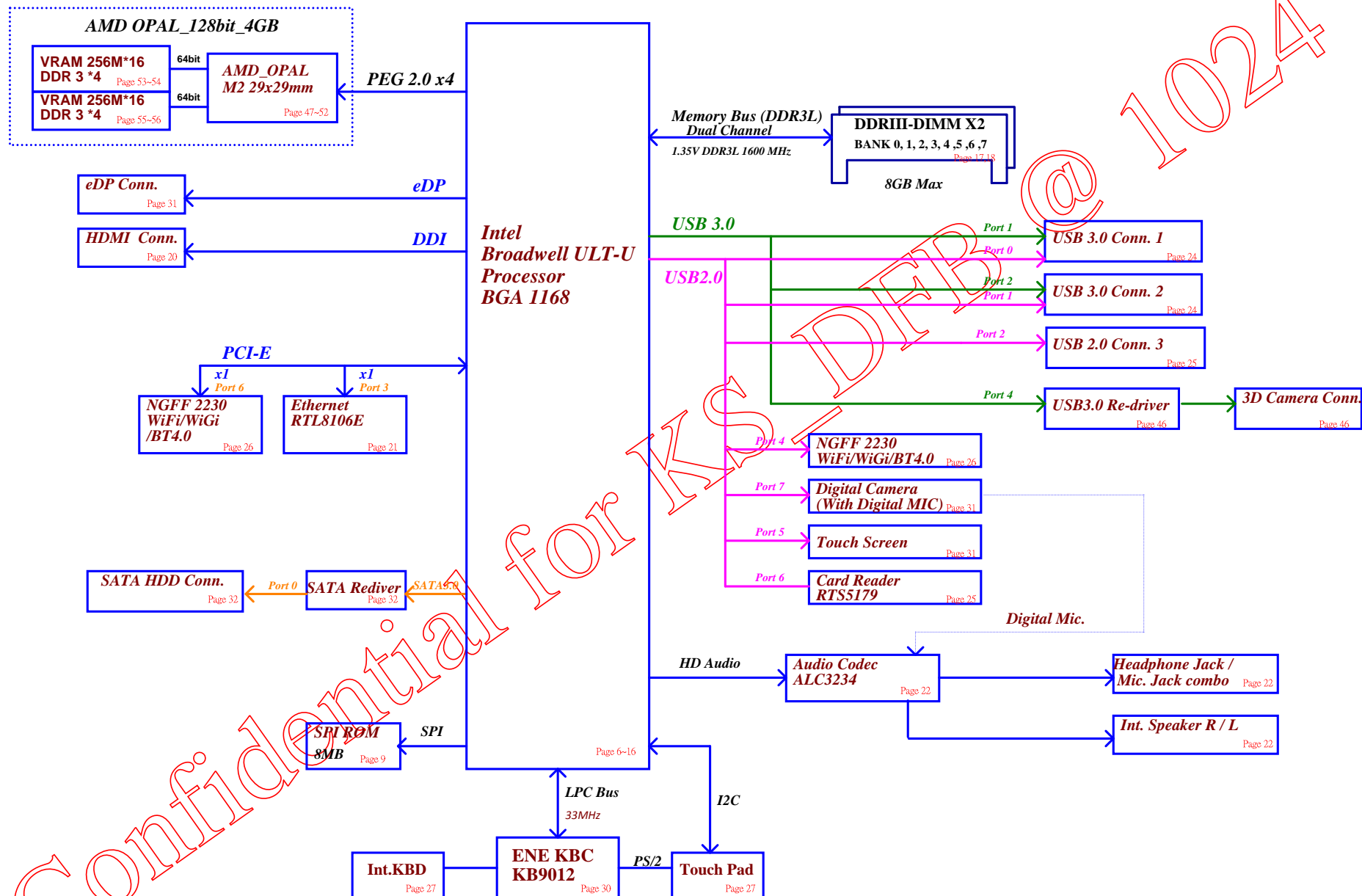
MODEL NAME : ZAVA1/ZAVC1  
PCB NO : DA80011D000 LA-B015P-R1.0

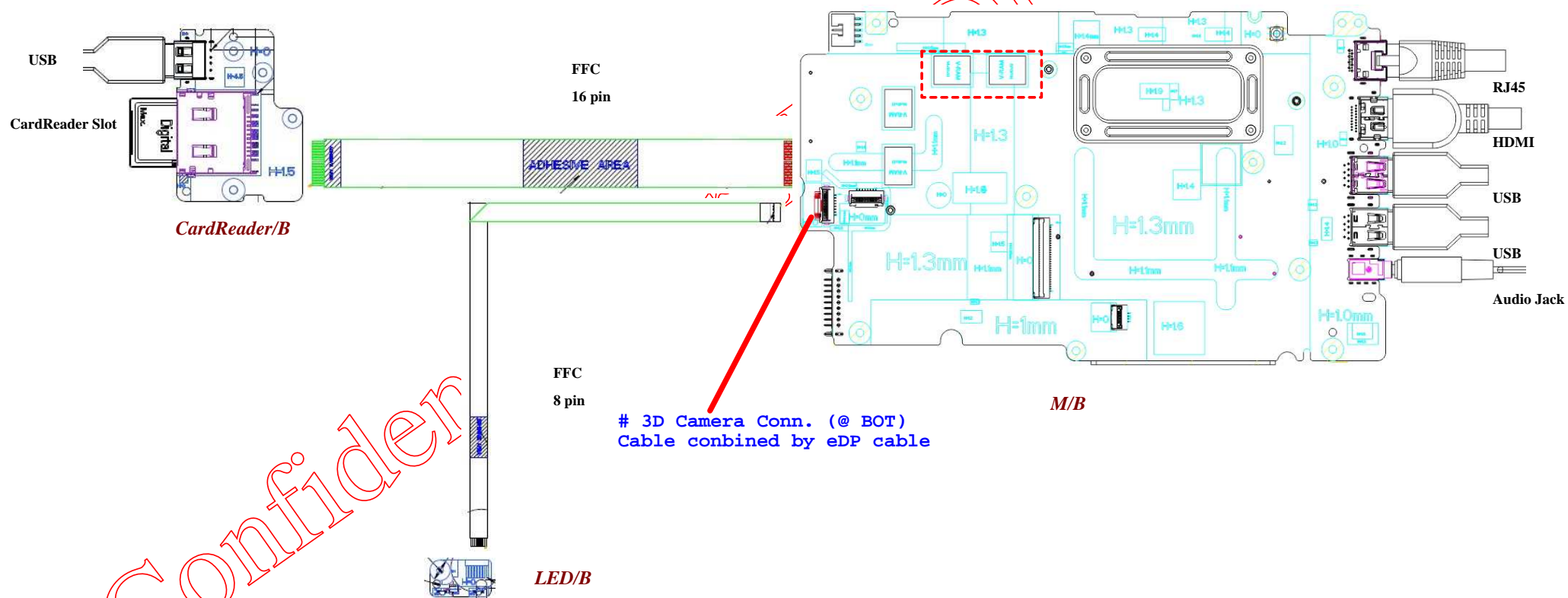
Compal Confidential  
Schematic Document

Intel BoardWell ULT  
ZAVA1/ZAVC1  
DIS AMD 25W/M2+DDR3x8

2014-10-17      Rev: 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2018/04/30	Title	Cover Page
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				LA-B015P	1.0
				Date	Friday, October 17, 2014
				Sheet	1 of 56





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Issued Date	2014/10/17	Deciphered Date	2018/04/30	MB/DB Drawing	
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				LA-B015P	1.0
Date: Friday, October 17, 2014				Sheet	3 of 56

## Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XD	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V			V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI 3D CAM			
7		PT(BDW) SSI 3D CAM		
8			PT(BDW) SSI 3D CAM	
9	ST(BDW) PT 3D CAM			
10		ST(BDW) PT 3D CAM		
11			ST(BDW) PT 3D CAM	
12	1.0(BDW) ST 3D CAM			
13		1.0(BDW) ST 3D CAM		
14			1.0(BDW) ST 3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL ( Diff. 100MHz )

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	3D Camera

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	

SATA

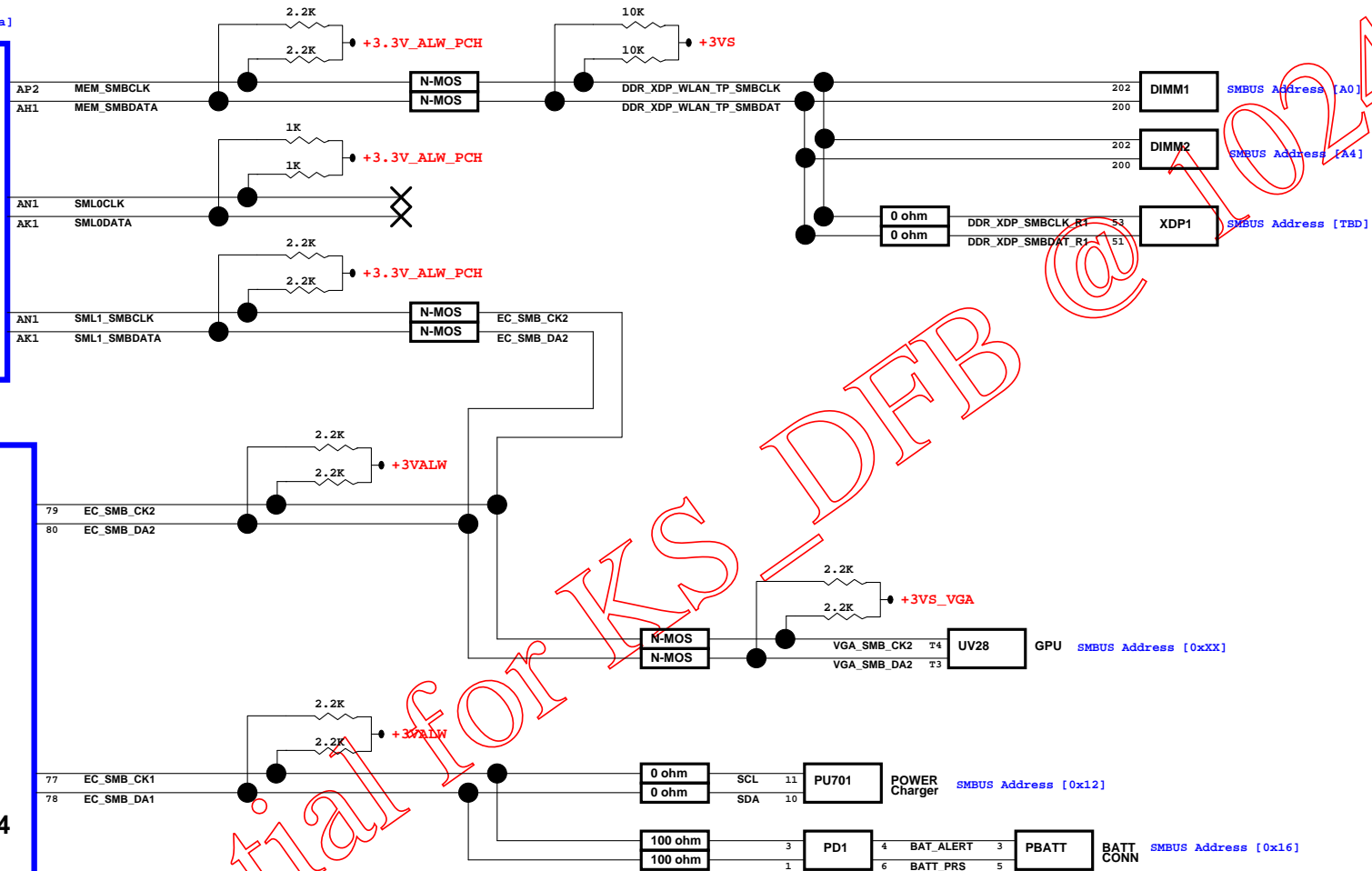
SATA0	HDD
SATA1	
SATA2	
SATA3	

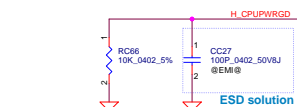
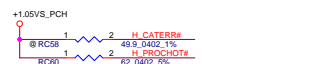
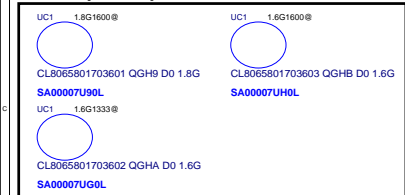
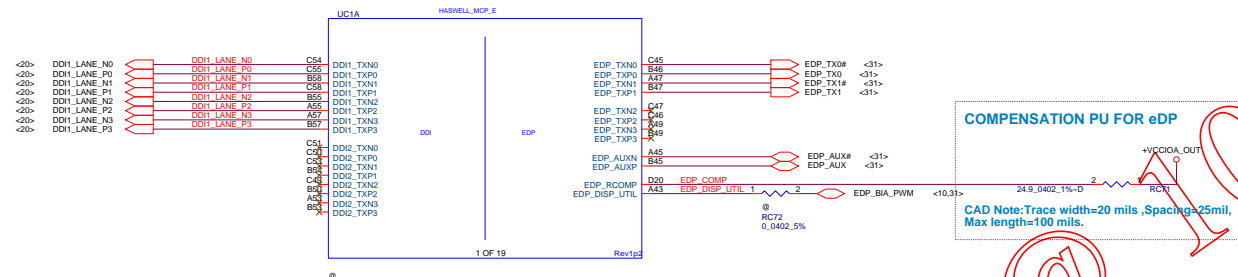
Symbol Note:

 : means Digital Ground : means Analog Ground

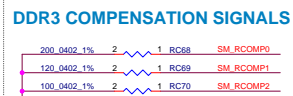
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		Date	Friday, October 17, 2014
		Sheet	4 of 56

SMBUS Address [0x9a]

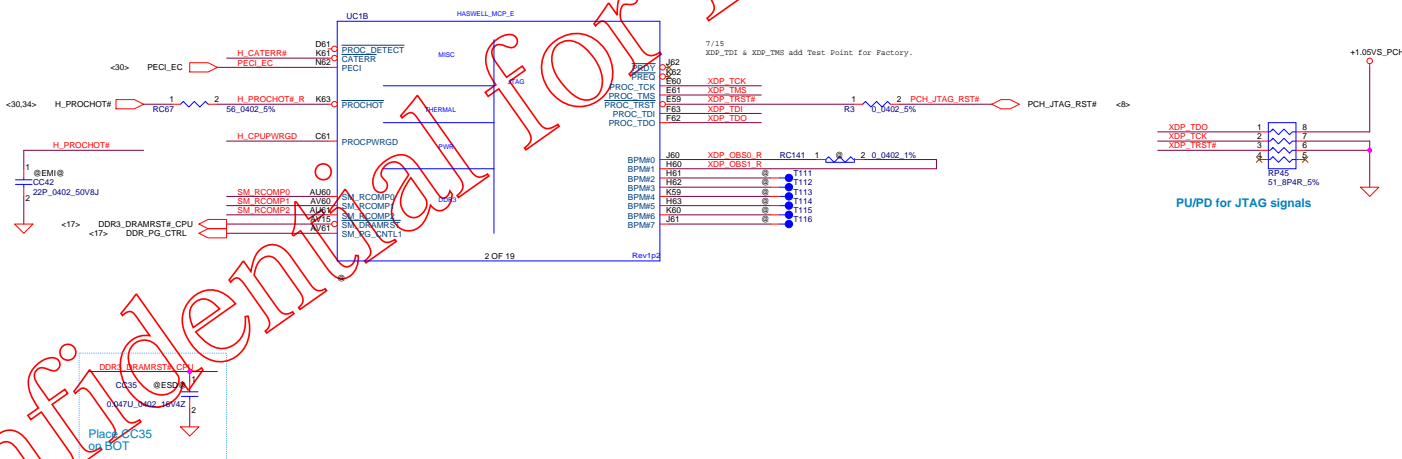
MCH  
Shark bayKBC  
KB9012A4



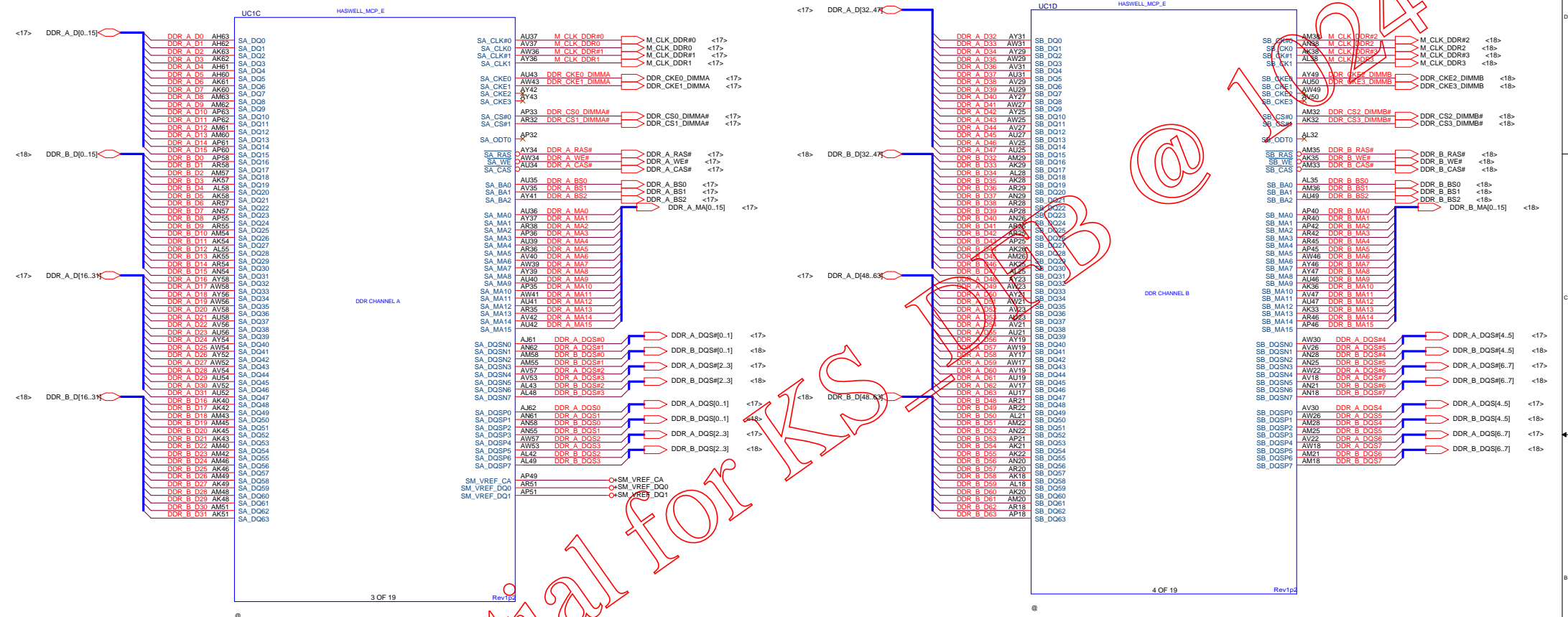
**CAD Note:**  
Avoid stub in the PWRGD path  
while placing resistors RC115



**CAD Note:**  
Trace width=12~15 mil, Spcing=20 mils  
Max trace length= 500 mil



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Date	Friday, October 17, 2014			Sheet	6 of 06

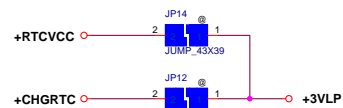
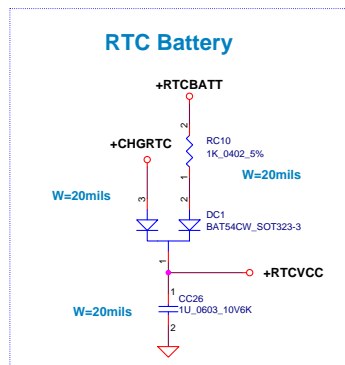


Confidential for KS

confirm by intel request PDG P141

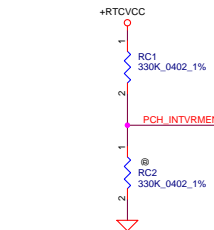
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	MCP(3,4/19) DDR3
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				Date	Wednesday, September 10, 2014
				Sheet	7 of 56

## RTC Battery

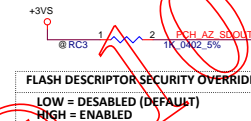


## For GCLK

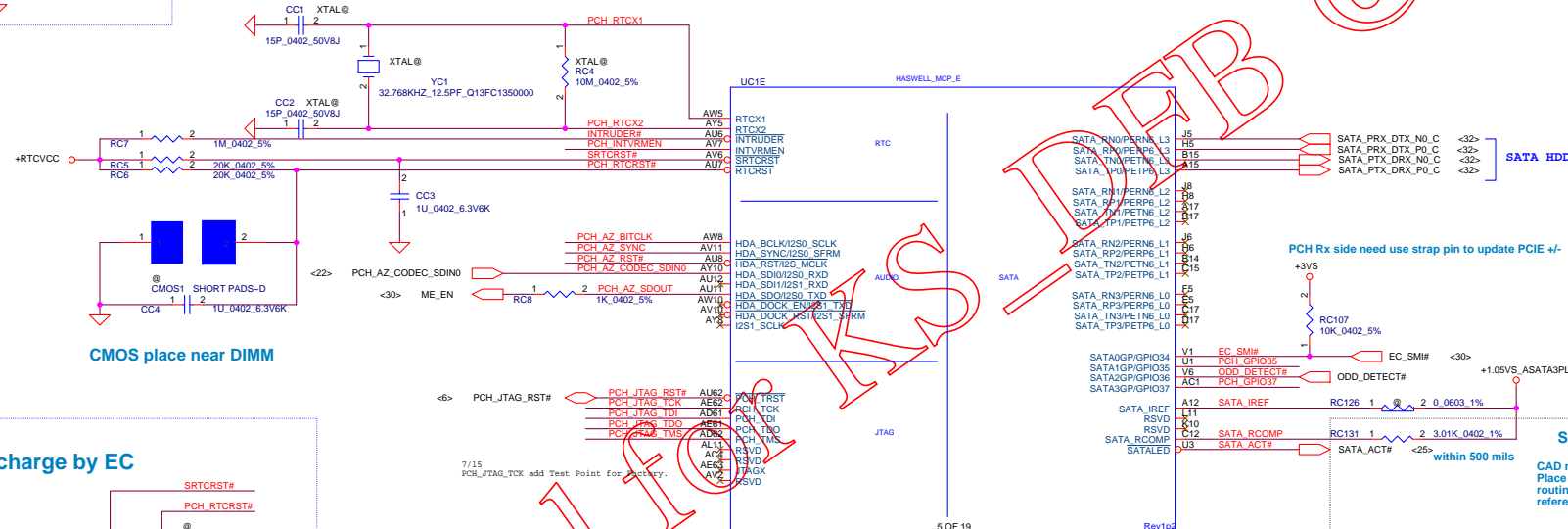
<19> PCH\_RTCX1



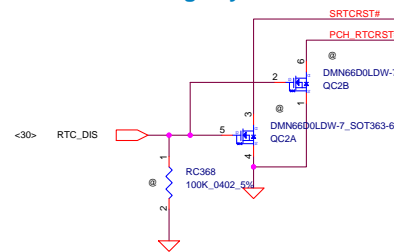
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs



FLASH\_DESCRIPTOR\_SECURITY\_OVERRIDE  
LOW = DISABLED (DEFAULT)  
HIGH = ENABLED



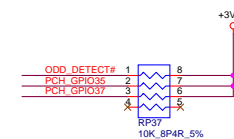
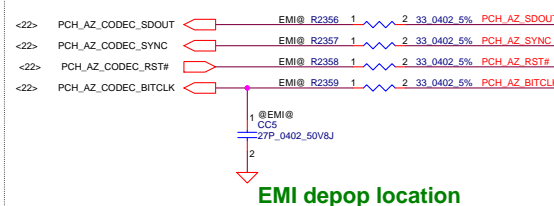
## RTC discharge by EC

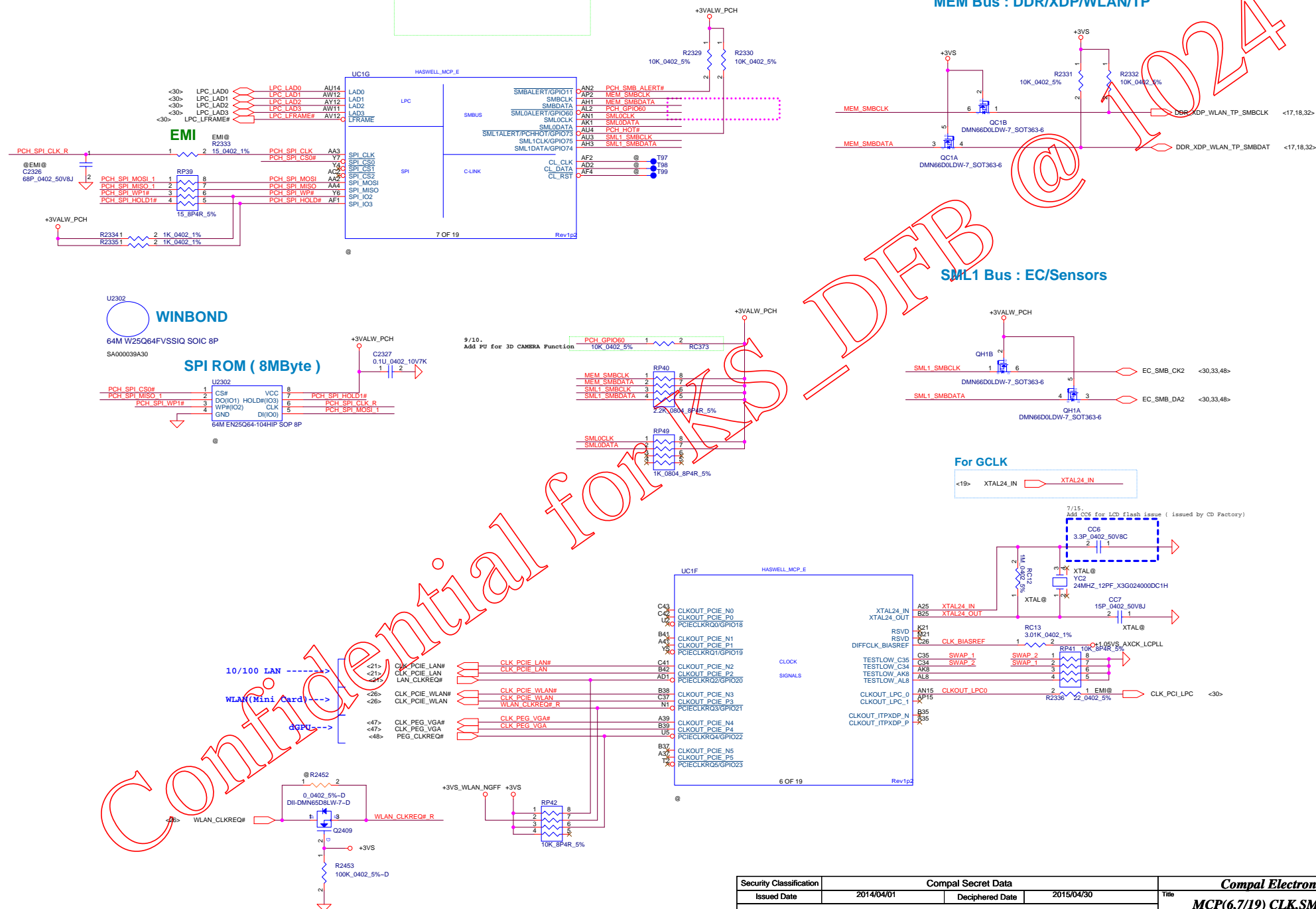


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

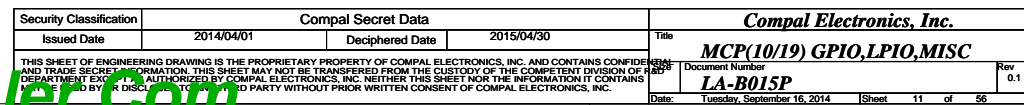
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

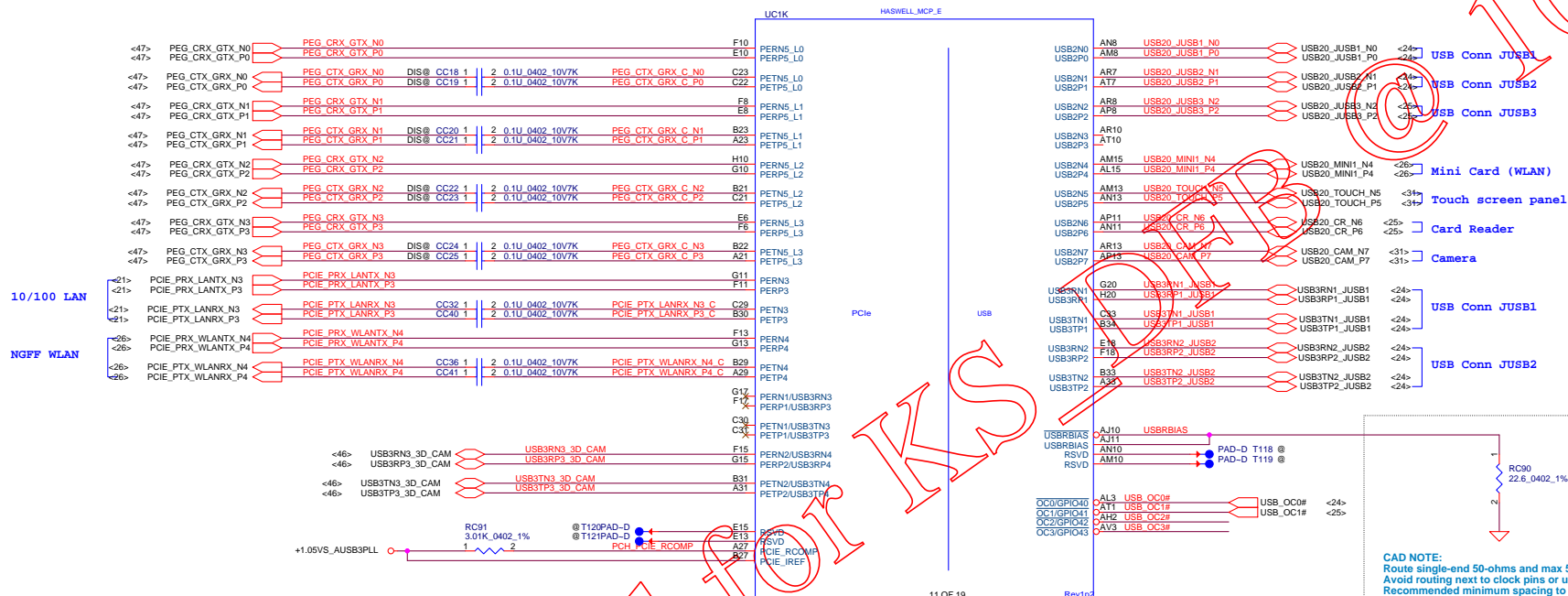
## HDA for Codec



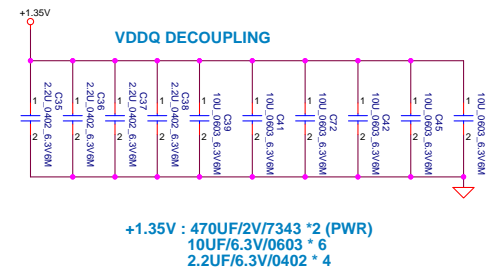
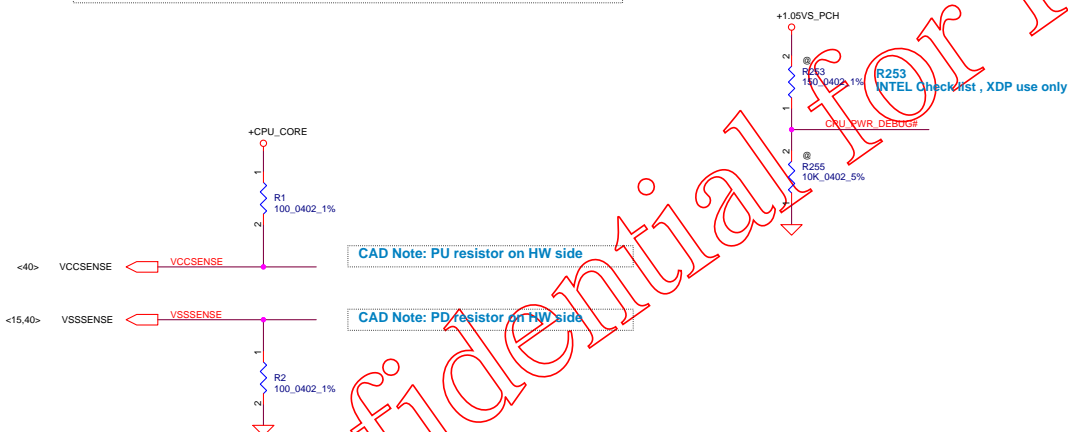
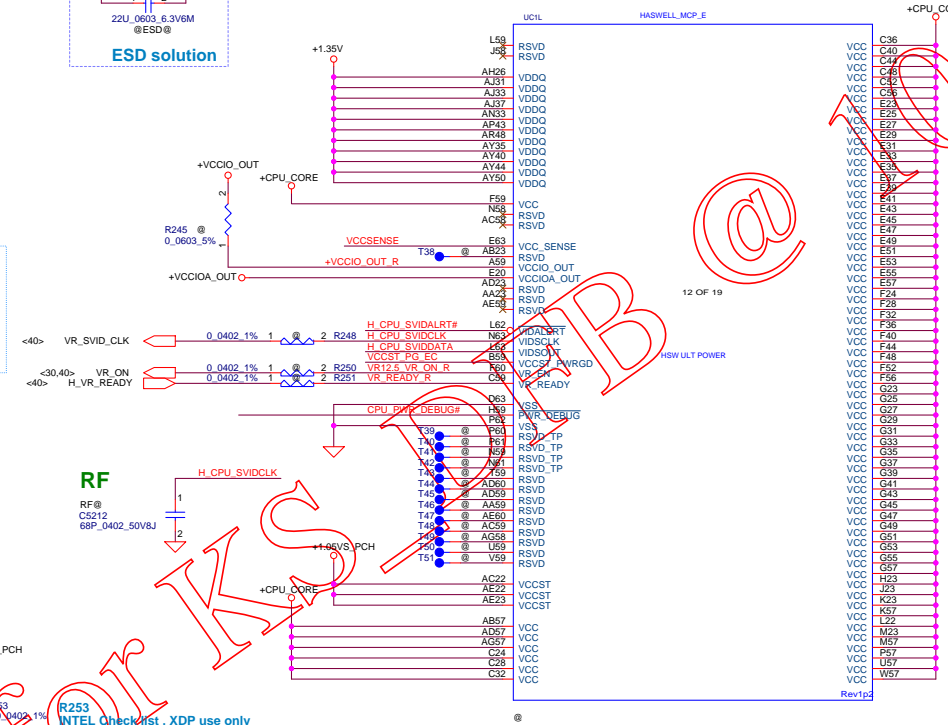
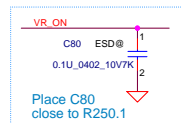
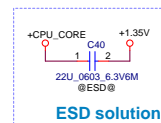




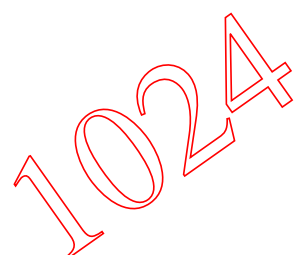




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				Date	Wednesday, September 10, 2014	Sheet







**CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU**

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				2015/04/30	
Title		MCP(14,15,16/19) VSS			
Document Number		LA-B015P			
Date:		Wednesday, September 10, 2014		Sheet 15 of 56	

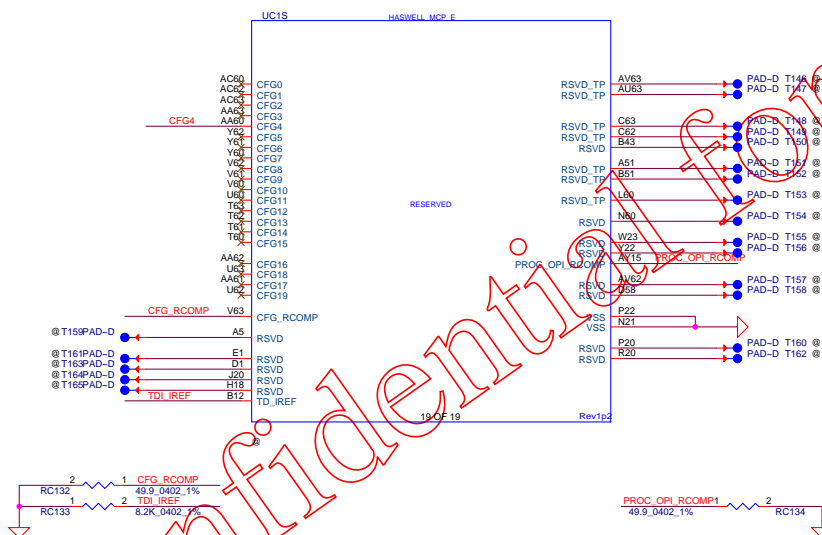
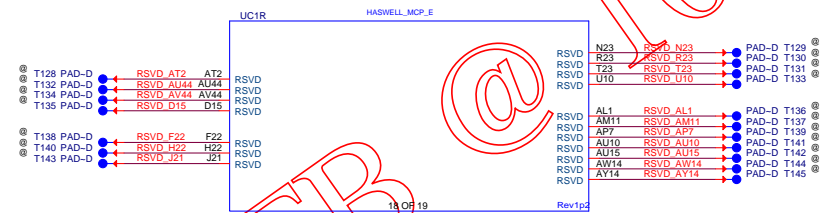


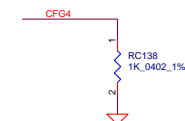
Diagram illustrating the RSVU (Redundant Signal Unit) architecture. The unit consists of two parallel paths of RSVD (Redundant Signal Value) inputs and outputs.

**Top Path:**

- RSVD N23, R23, T23, U10 (Inputs)
- RSVD N23, R23, T23, U10 (Intermediate Signals)
- PAD-D T129, PAD-D T130, PAD-D T131, PAD-D T133 (Outputs)

**Bottom Path:**

- RSVD AL1, AM11, AP7, AU10, AU16, AW14, AY14 (Inputs)
- RSVD AL1, AM11, AP7, AU10, AU16, AW14, AY14 (Intermediate Signals)
- PAD-D T136, PAD-D T137, PAD-D T139, PAD-D T141, PAD-D T142, PAD-D T144, PAD-D T145 (Outputs)



Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

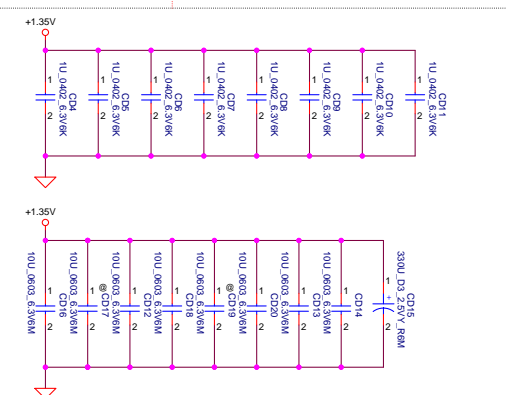
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<7> DDR\_A\_DQ(0..63)  
<7> DDR\_A\_DQS(0..7)  
<7> DDR\_A\_MA(0..15)

All VREF traces should have 10 mil trace width

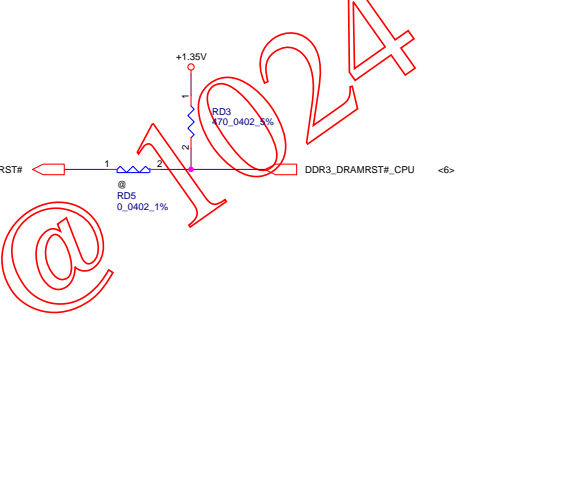
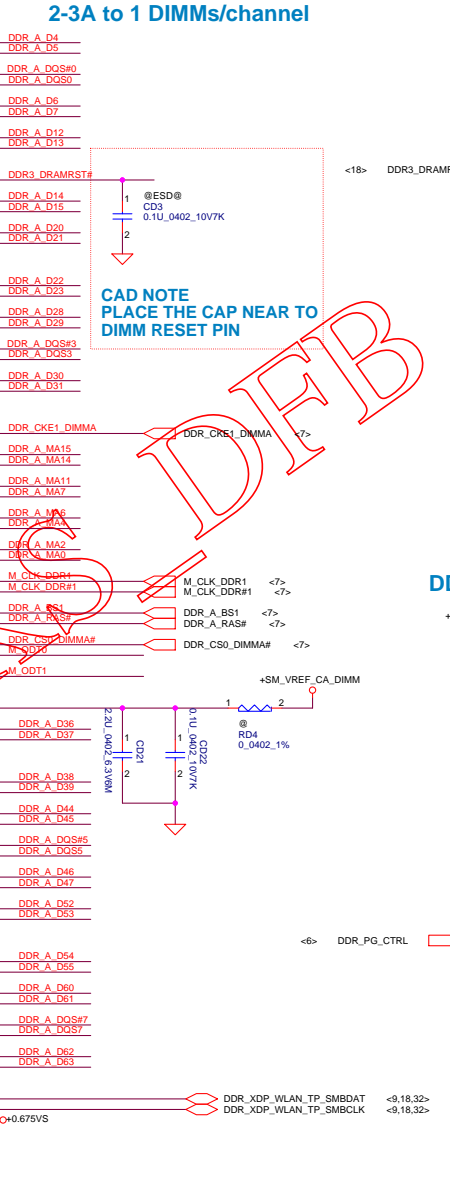
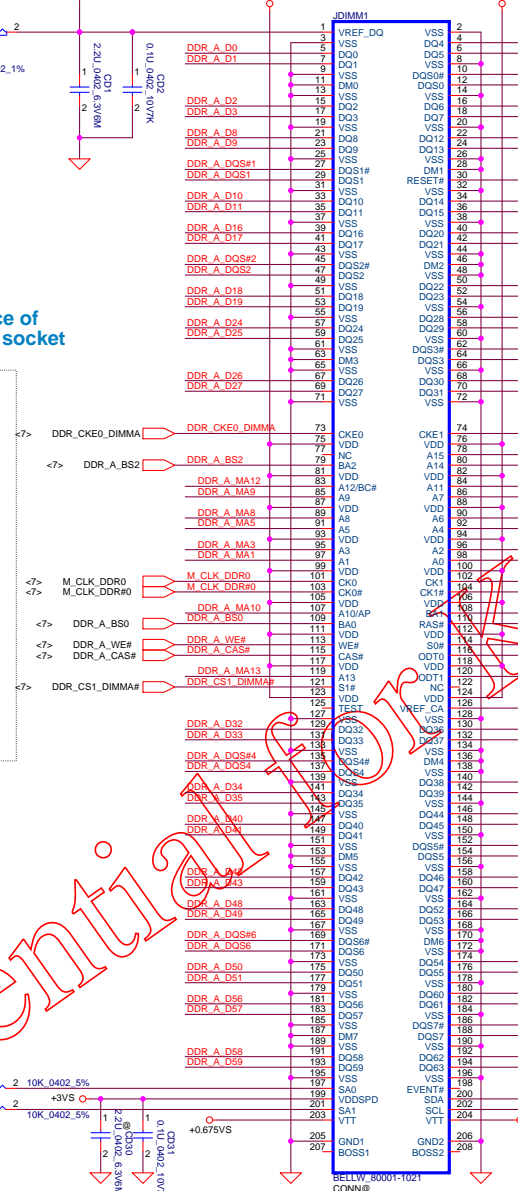
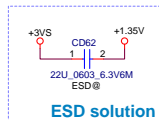
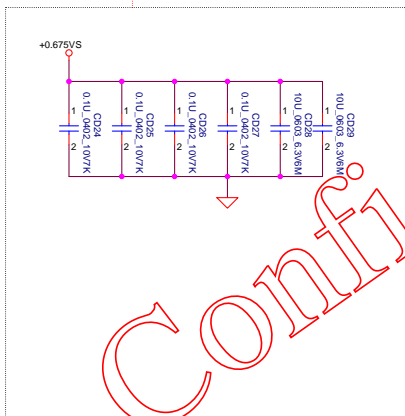
Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

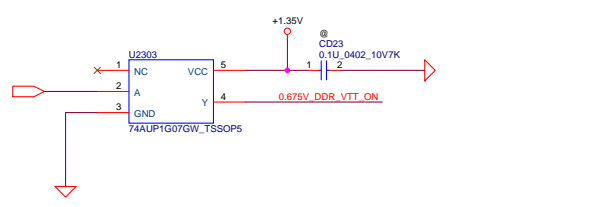
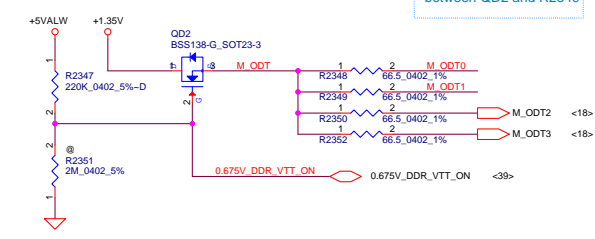
CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN

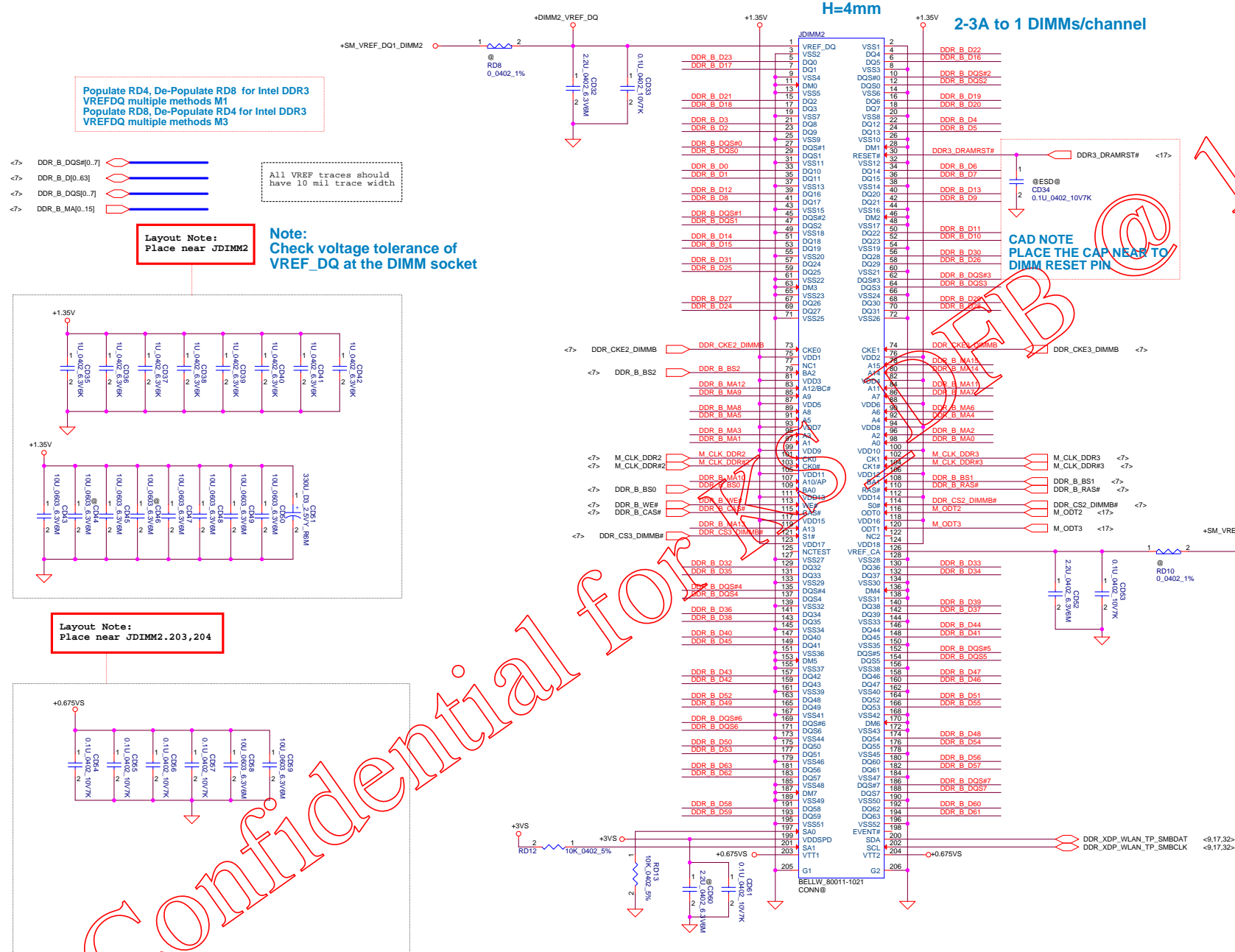


Layout Note:  
Place near JDIMM1.203,204

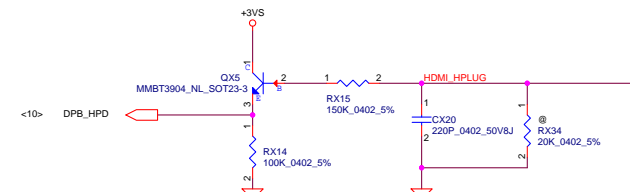
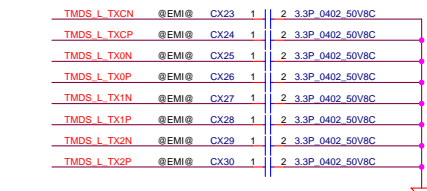
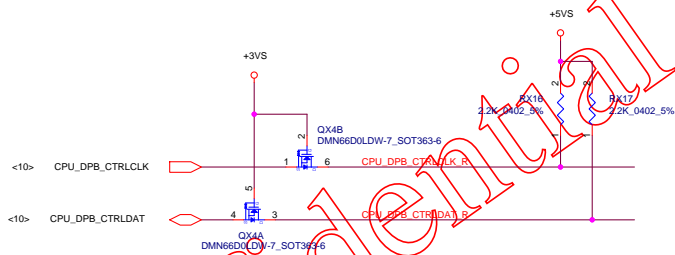
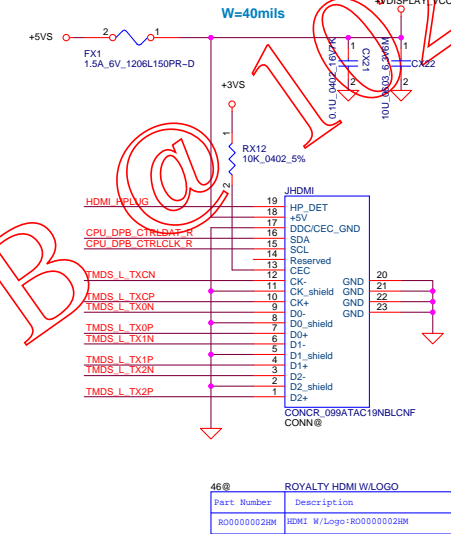
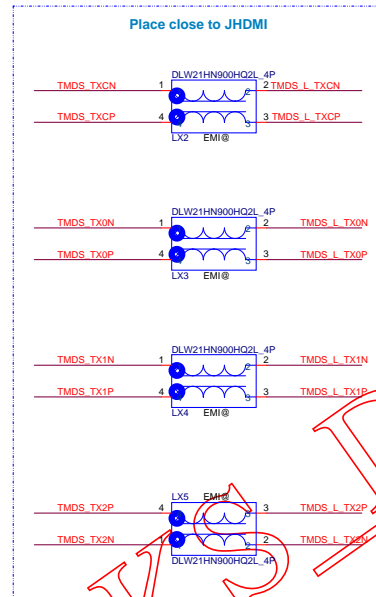
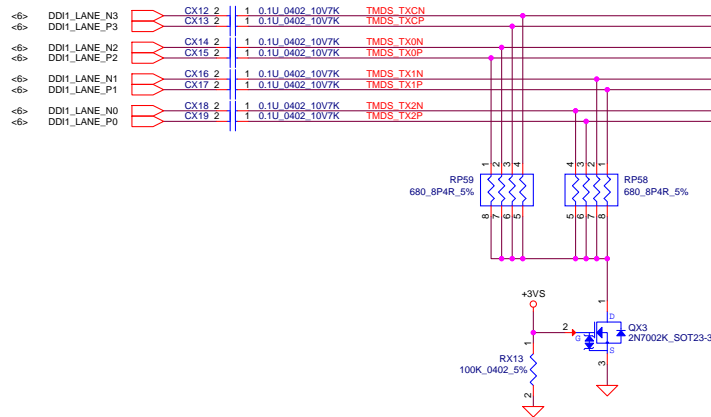


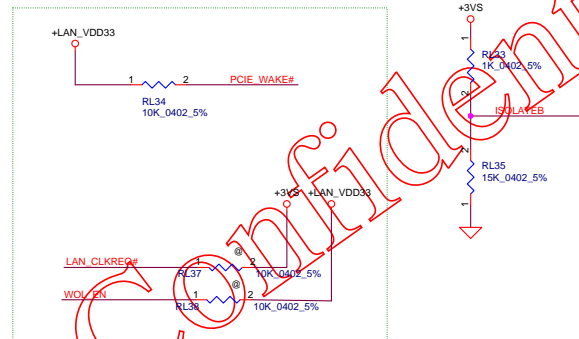
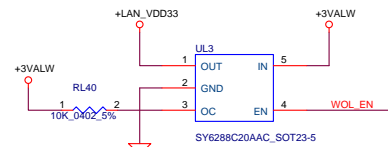
DDR3L SODIMM ODT GENERATION



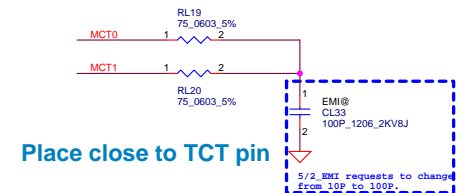
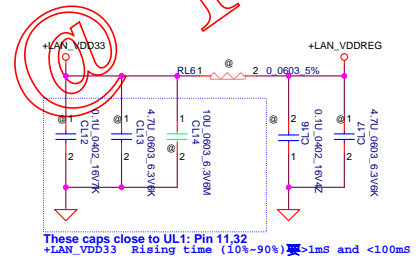
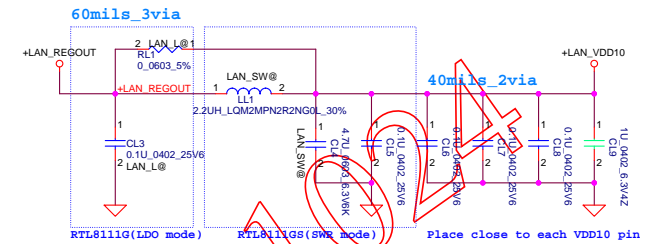




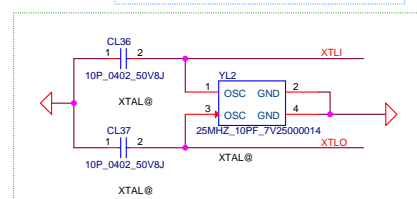




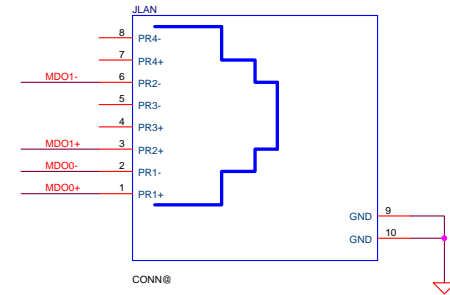
## Reserve 10K pull LAN\_IO



**Place close to TCT pin**



XTAL

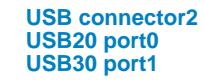
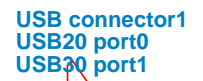


**WWW.AliSaler.Com**

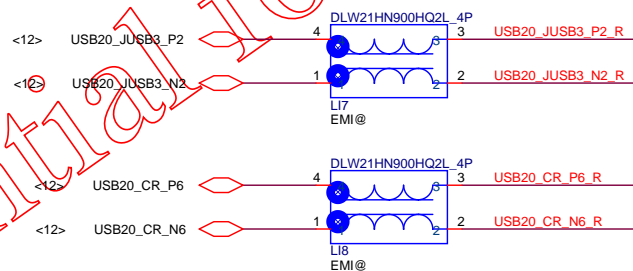
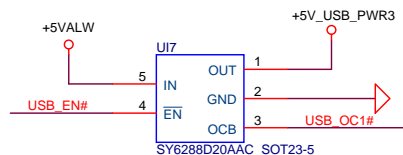
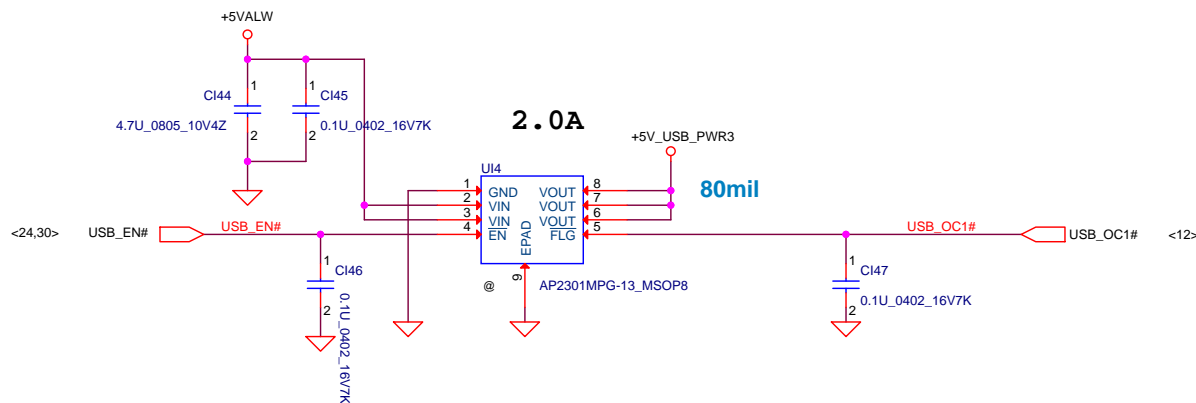


Confidential for KS\_DFB @ 1024

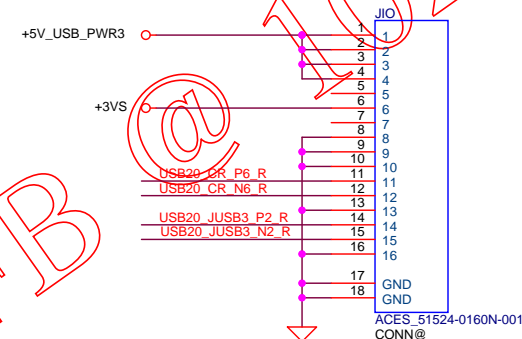
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Issued Date		Deciphered Date		Document Number	
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				Sheet 23 of 56	
				Rev 0.1	



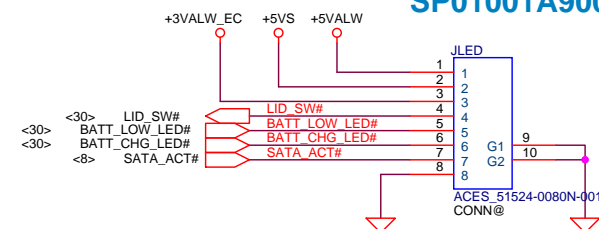
**WWW.AliSaler.Com**



IO to MB CONN  
Substitute: SP01001FS00

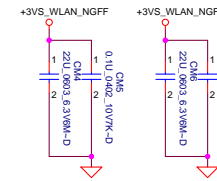
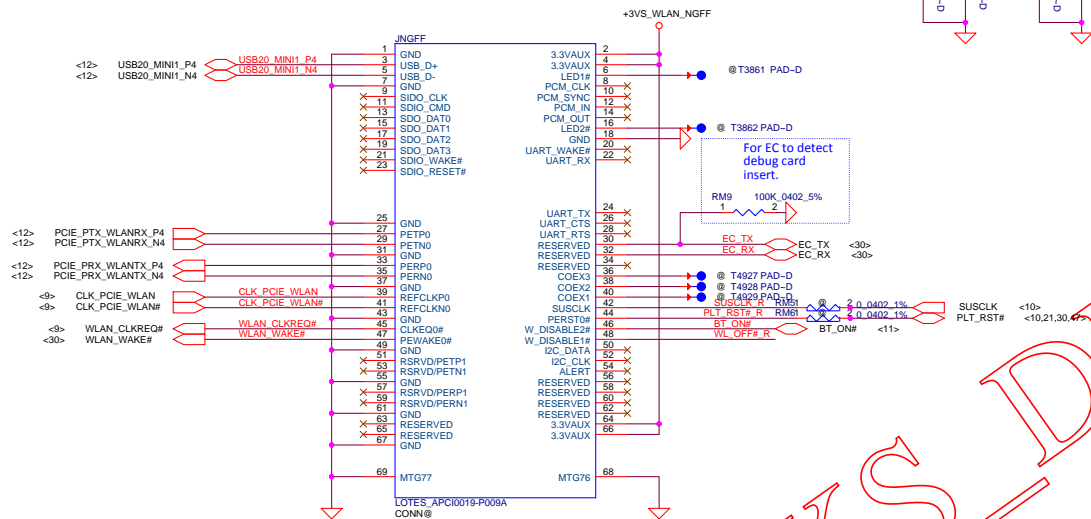


LED/B TO M/B  
SP01001A900

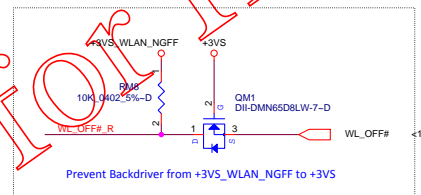
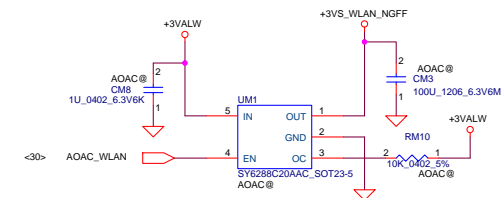
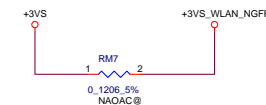



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				LA-B015P	0.1
Date: Tuesday, September 16, 2014				Sheet	25 of 56

closed to pin 2, 4                  closed to pin 64, 66



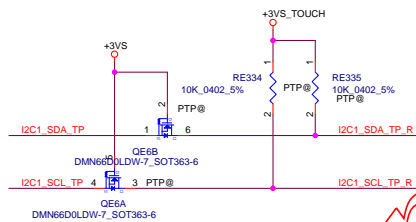
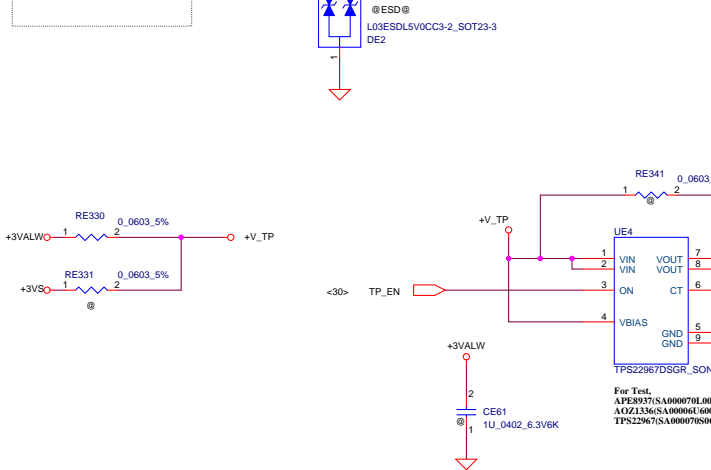
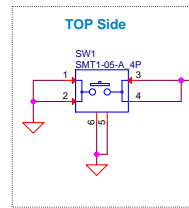
**+3VALW TO +3VS\_WLAN\_NGFF**



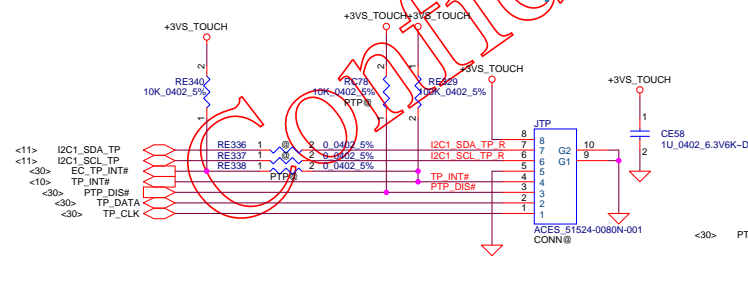
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>NGFF WLAN</b>	
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				Rev	0.1

## Power ON Circuit

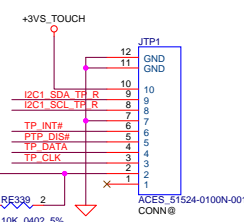
### ON/OFF switch



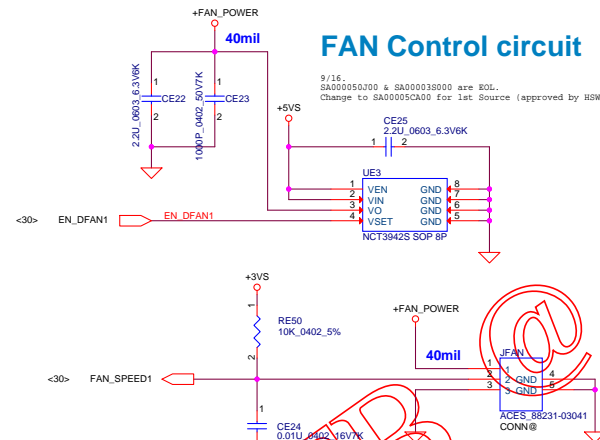
### Touch pad



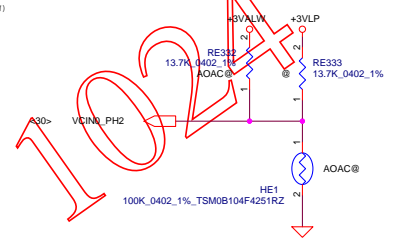
### PTP



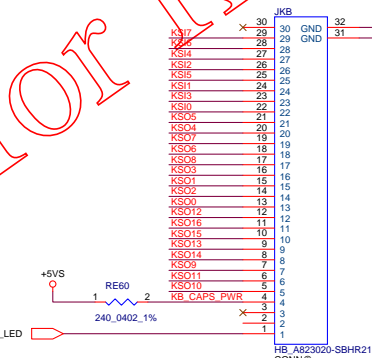
## FAN Control circuit



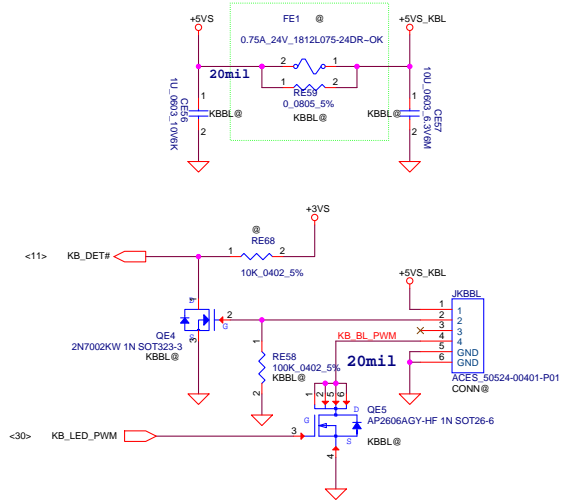
### HE1 place around FAN area.



## INT\_KBD Connector

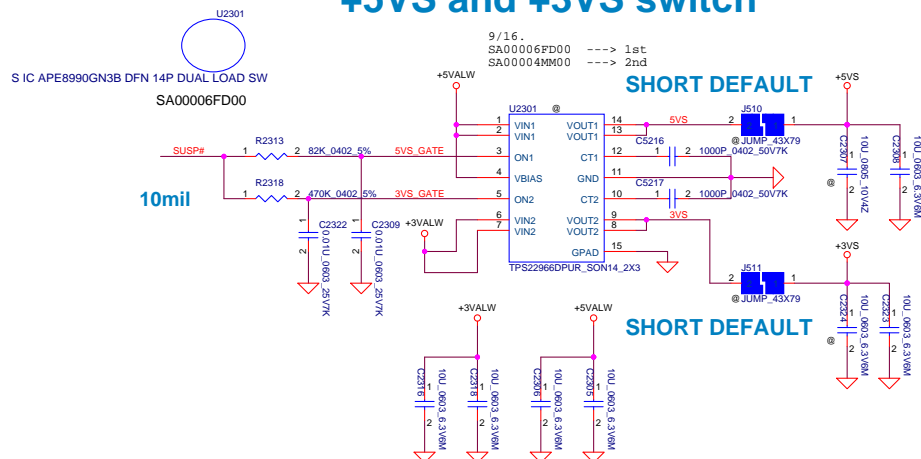


## \* Key Board Back Light

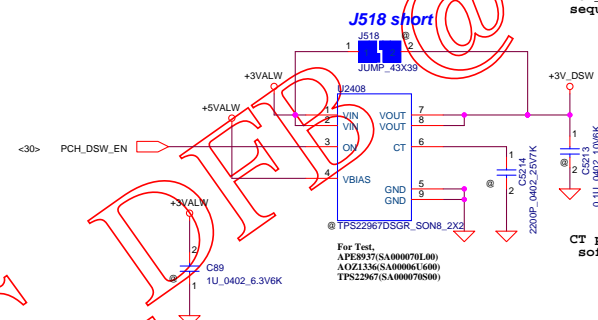


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Date				Friday, October 17, 2014	Sheet 27 of 56

## +5VS and +3VS switch

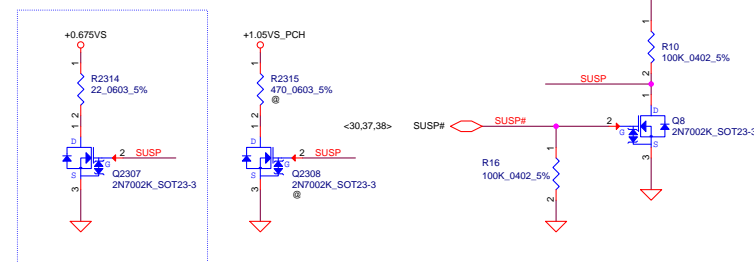
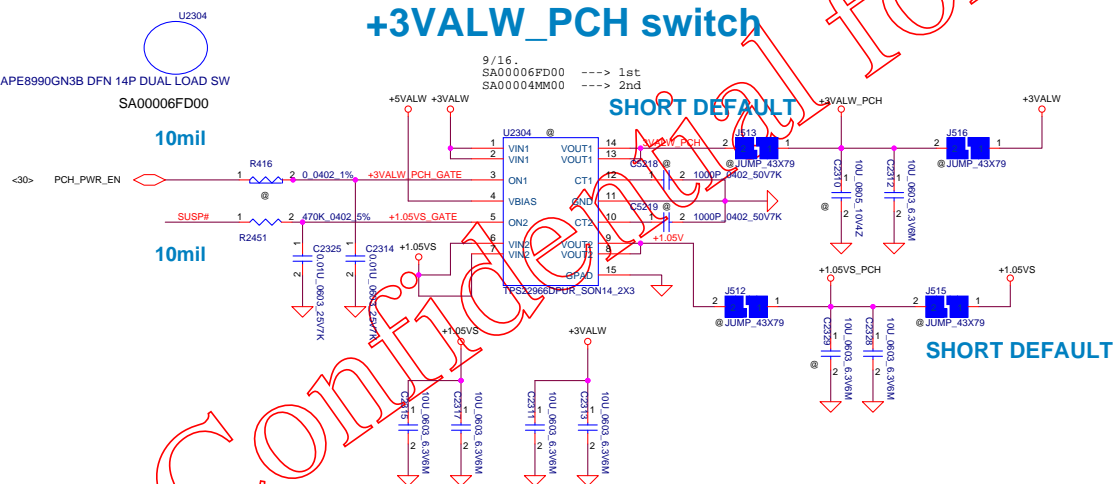


## +3VALW TO +3V\_DSW



+3V\_DSW have soft start sequence: +3V\_DSW stable > +3VALW\_PCH > 0ms

## +3VALW\_PCH switch



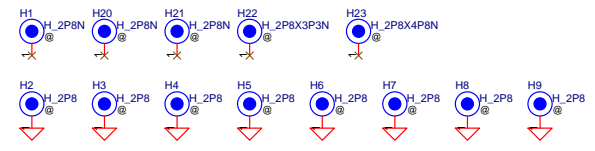
For Intel S3 Power Reduction

Security Classification	Compal Secret Data		Title	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	DC/DC Interface
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Date: Tuesday, September 16, 2014				Rev 0.1
Sheet 28 of 56				

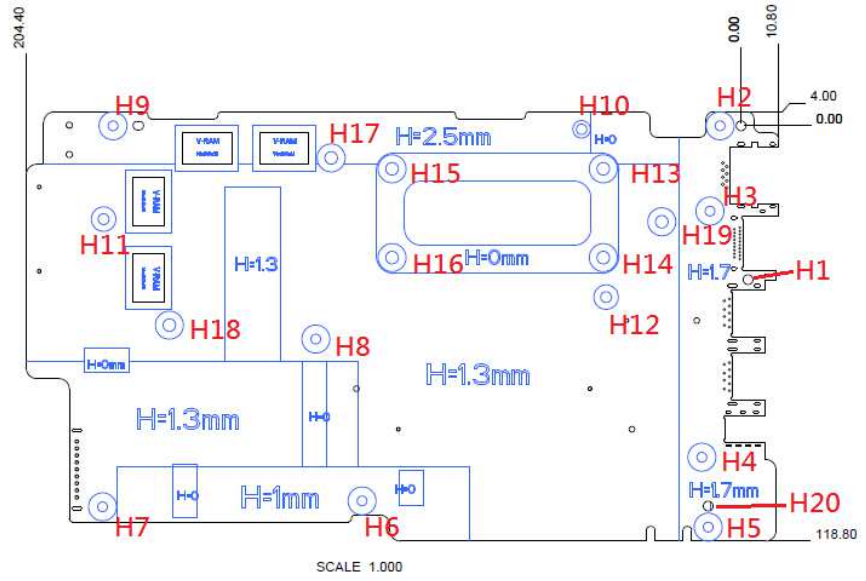
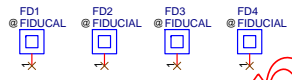
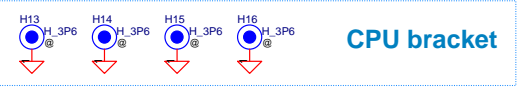
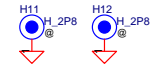
# Screw Hole

ZZZ  
PCB 13G LA-B015P REV0 M/B  
DA80011D000

1024



H10 Delete.  
Layout informed PCB vendor to do PTH solution.  
(Function is same as beofre.)

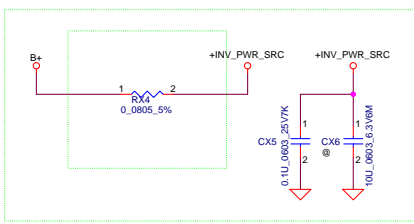
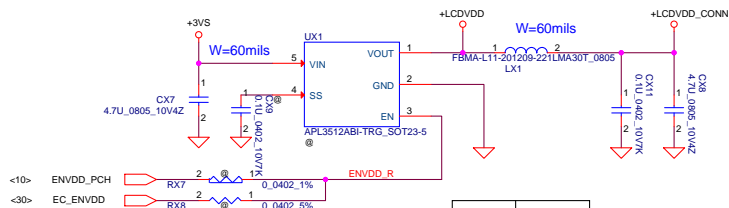
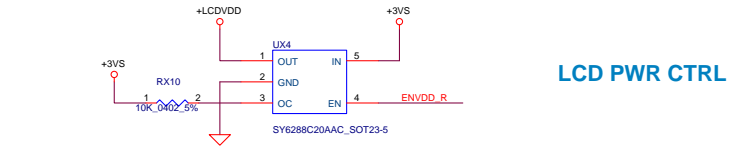


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				Date	Wednesday, September 10, 2014
				Sheet	29 of 56
				Rev	0.1

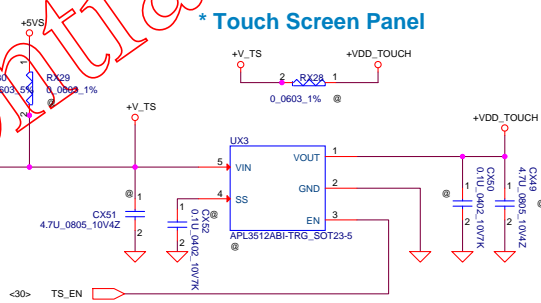


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				LA-B015P	
Date:	Friday, October 17, 2014	Sheet	30	of	56



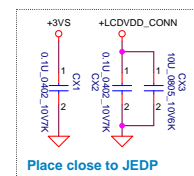
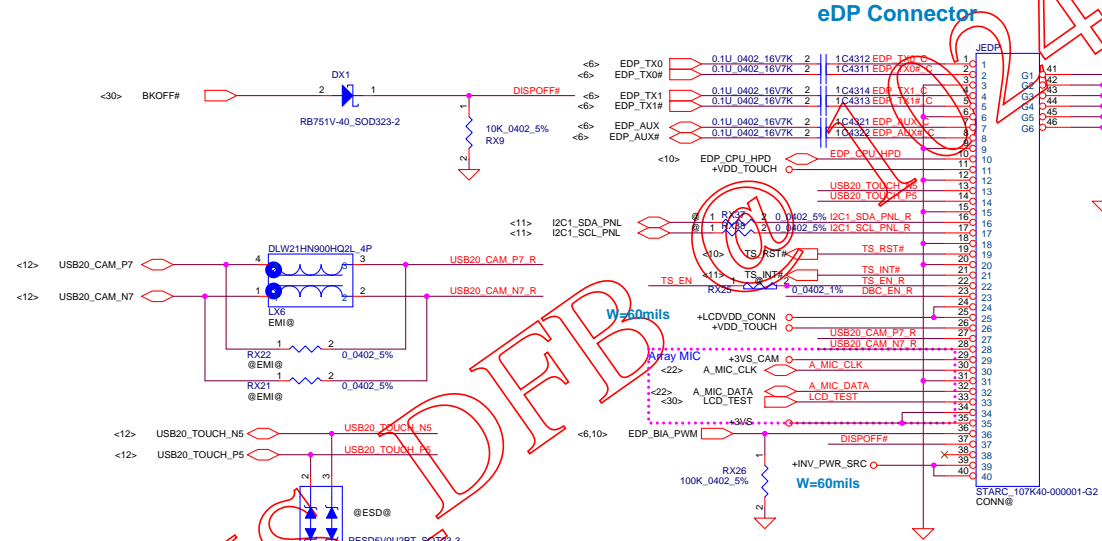
**\* Touch Screen Panel**

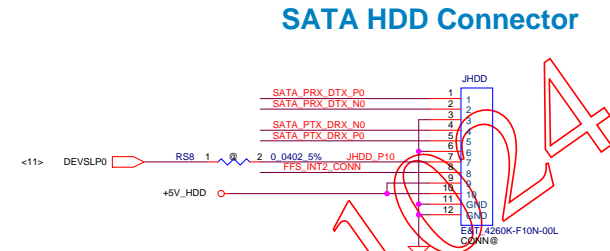
**Webcam PWR CTRL**



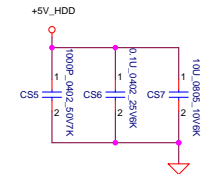
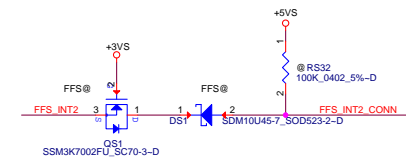
**SS table**

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

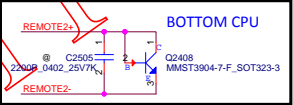
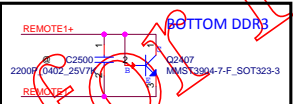
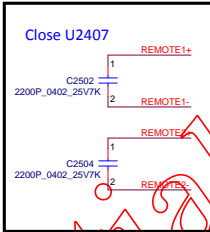
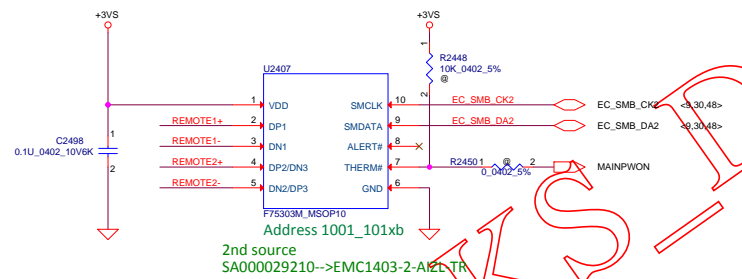




## SHORT DEFAULT

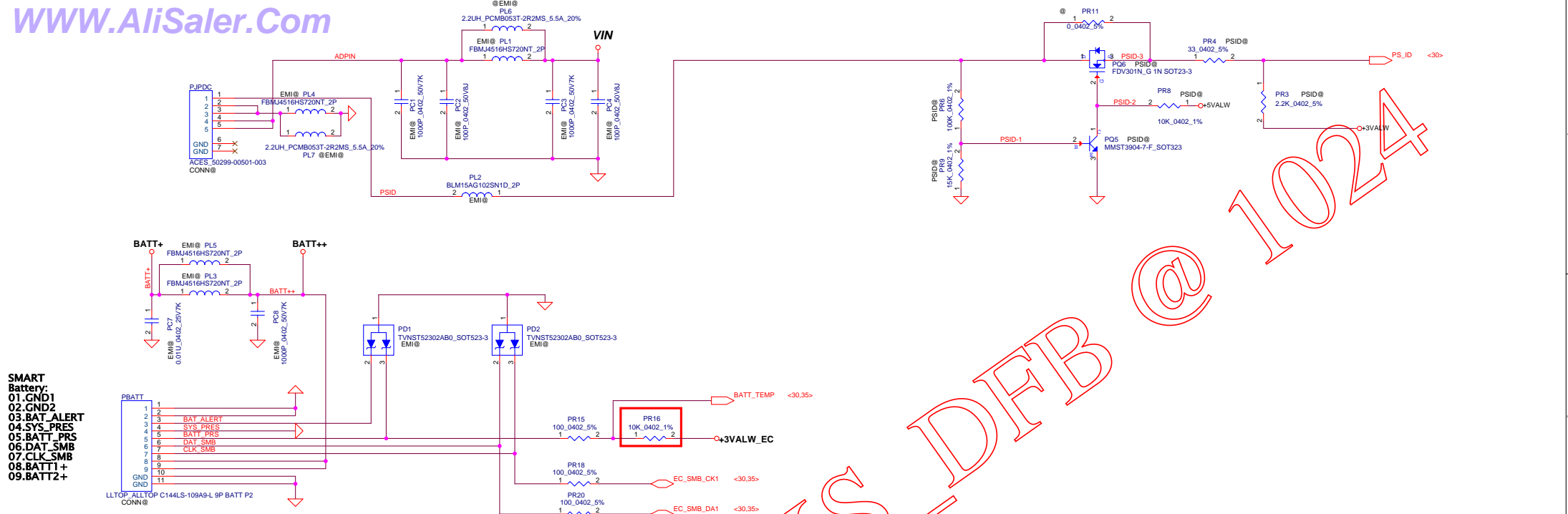
[illegible]

Fintek thermal sensor  
placed near by TOP DDR3



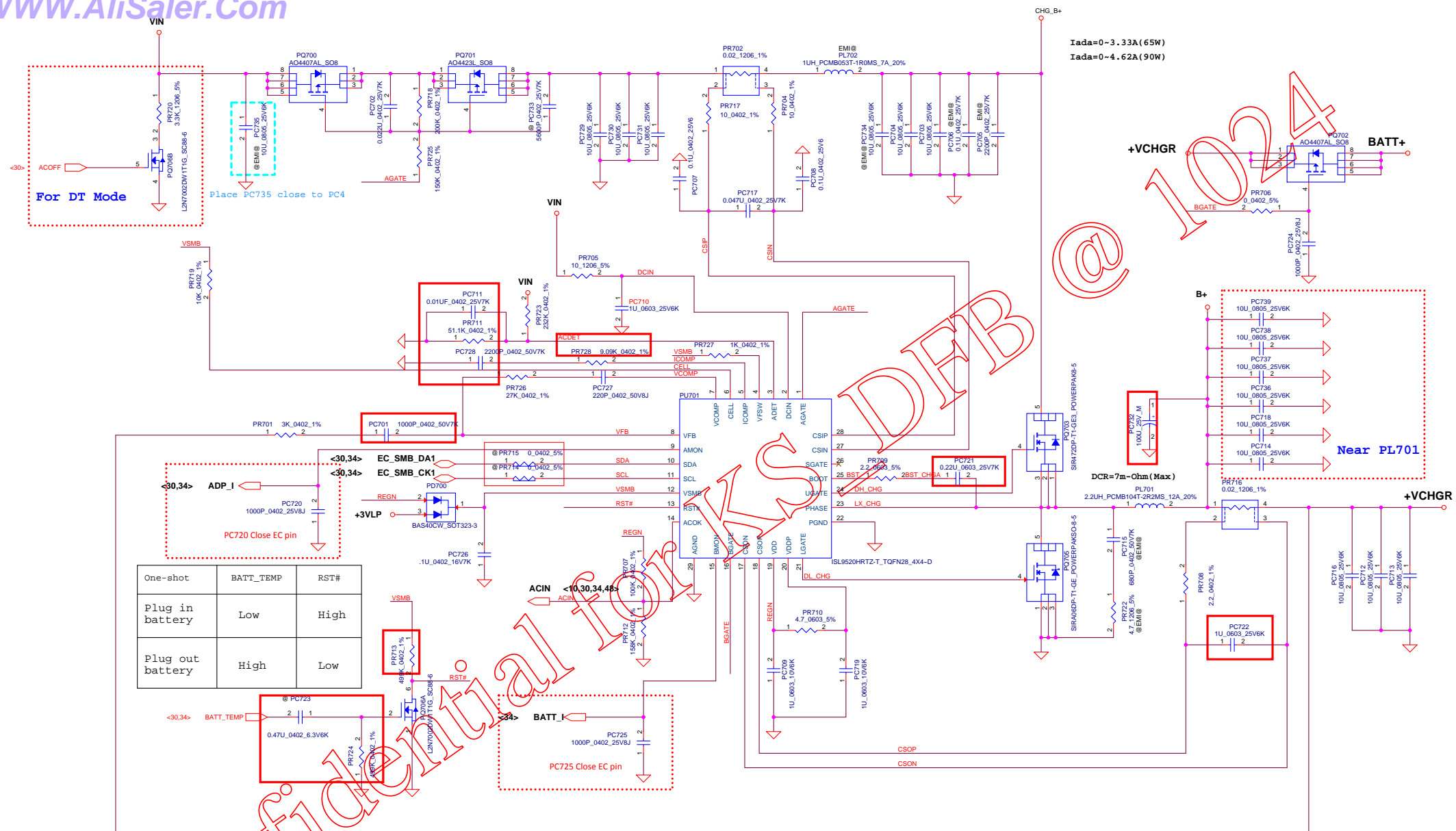
REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

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			LA-B015P	0.1
			Date: Wednesday, September 10, 2014	Sheet 33 of 56

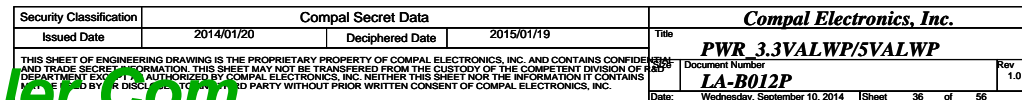


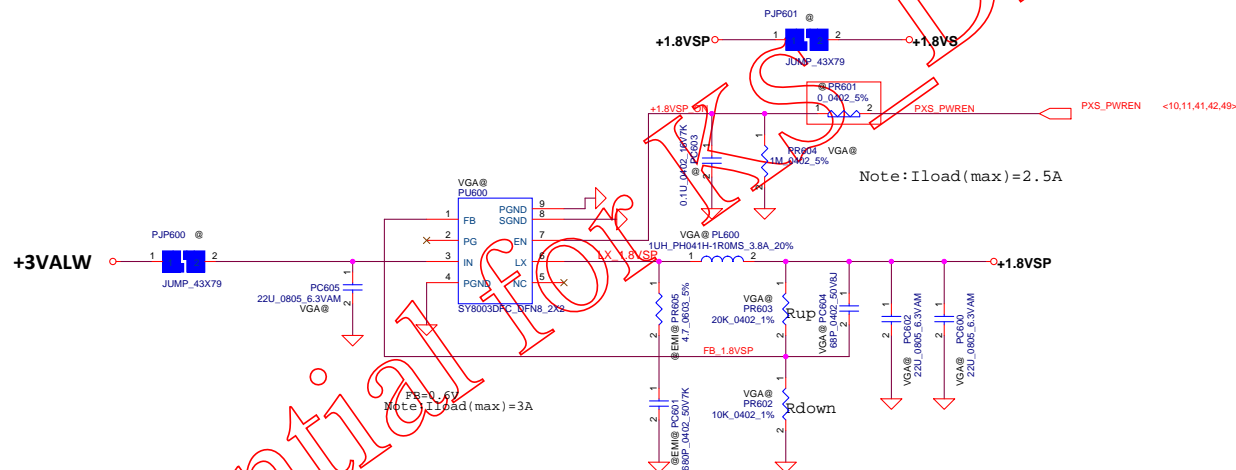
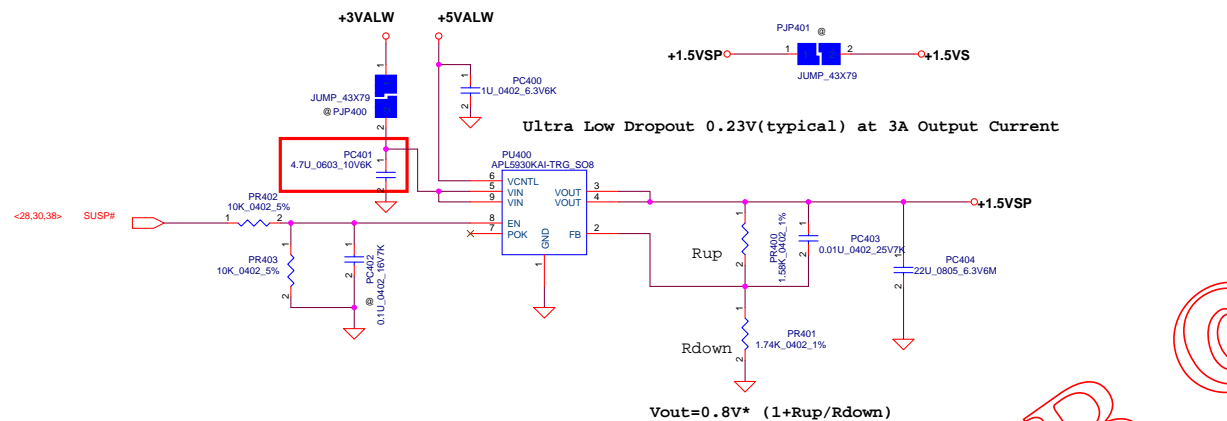
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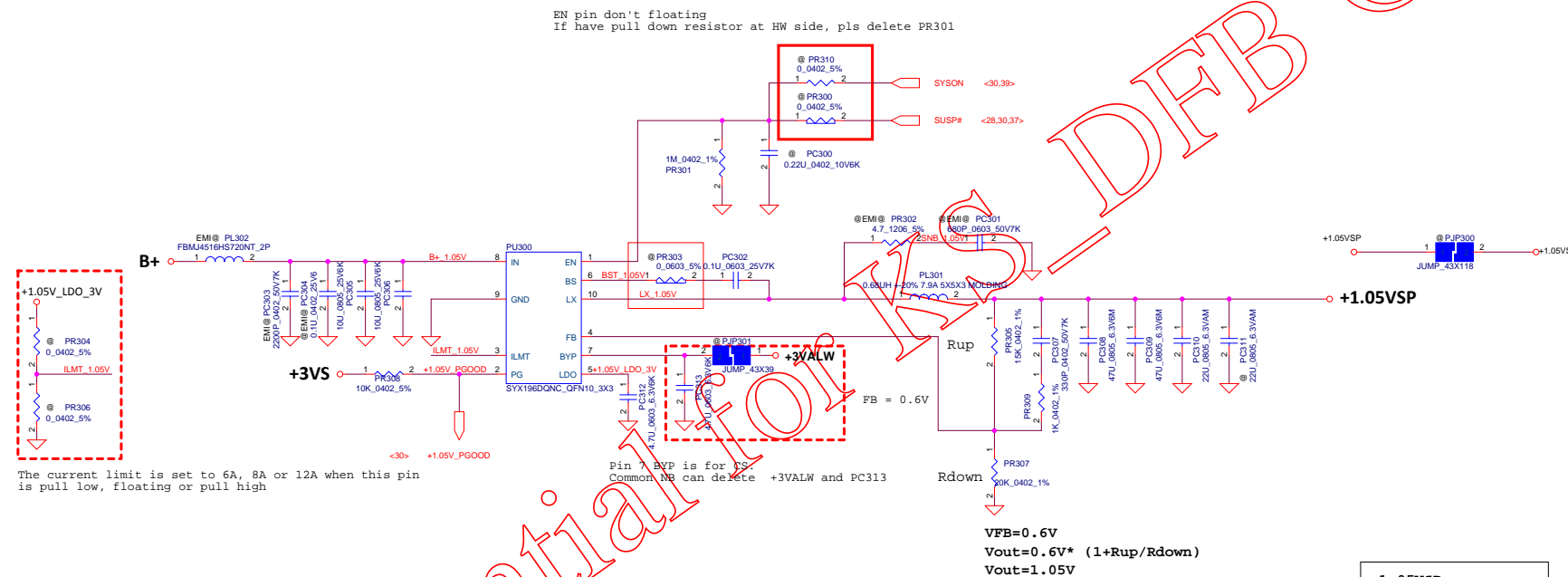
for S/D E B



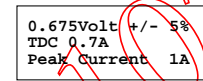
**2S2P : CV = 8.4V CC = 3.9A**  
**3S1P : CV = 12.6V CC = 2A**

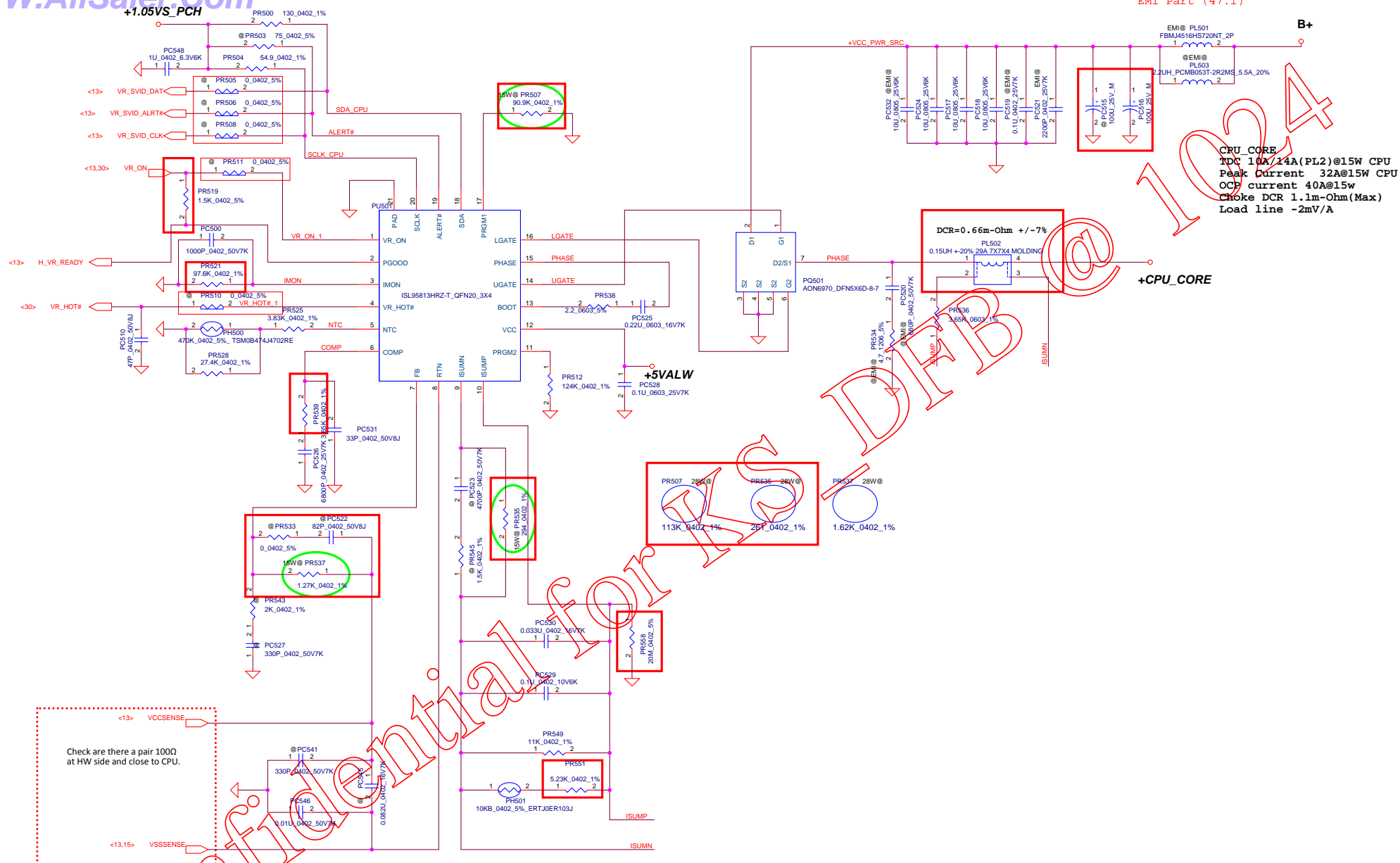


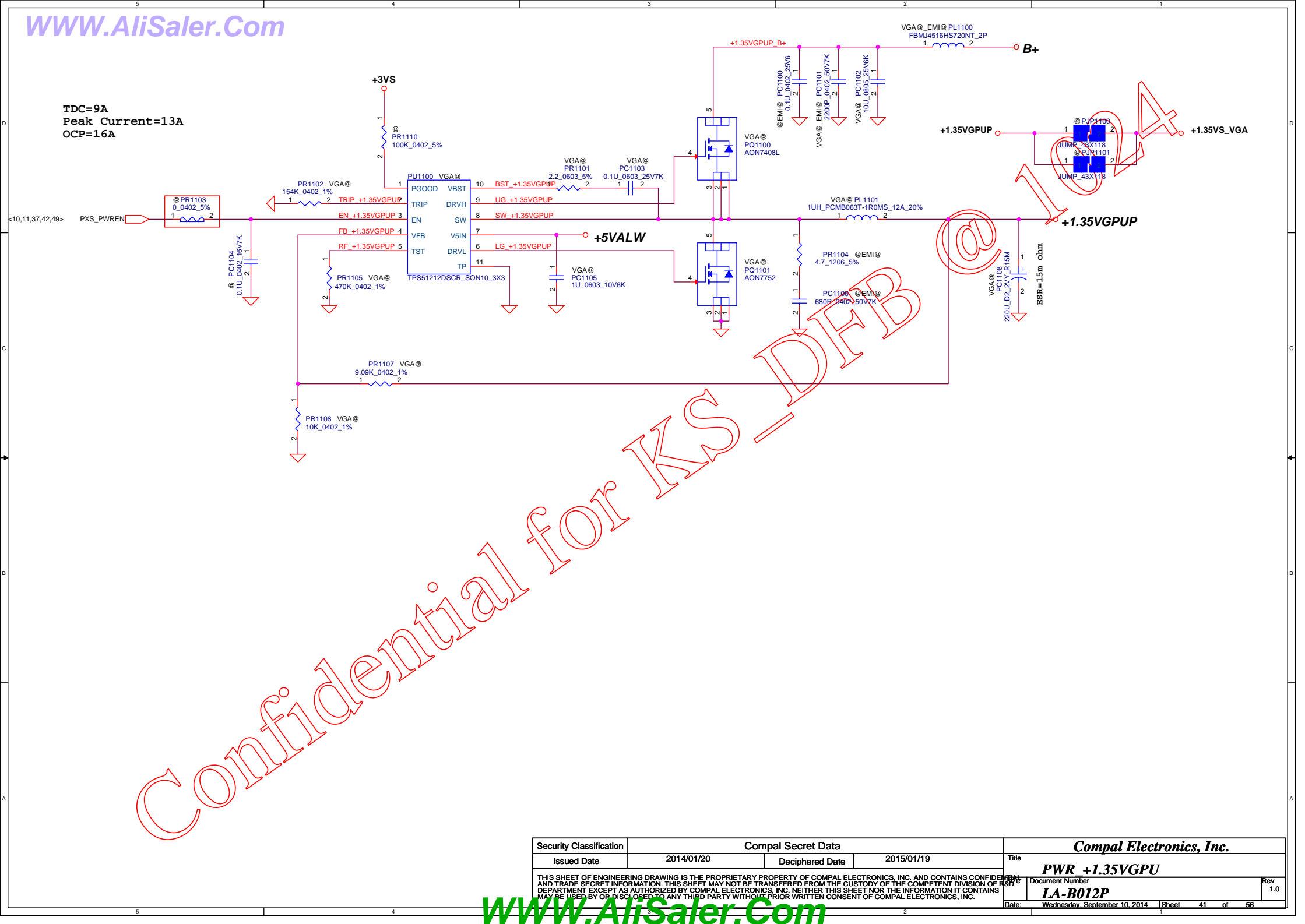


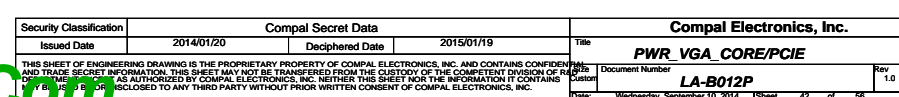


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				LA-B012P
				Rev 1.0
				Date: Wednesday, September 10, 2014   Sheet 38 of 56





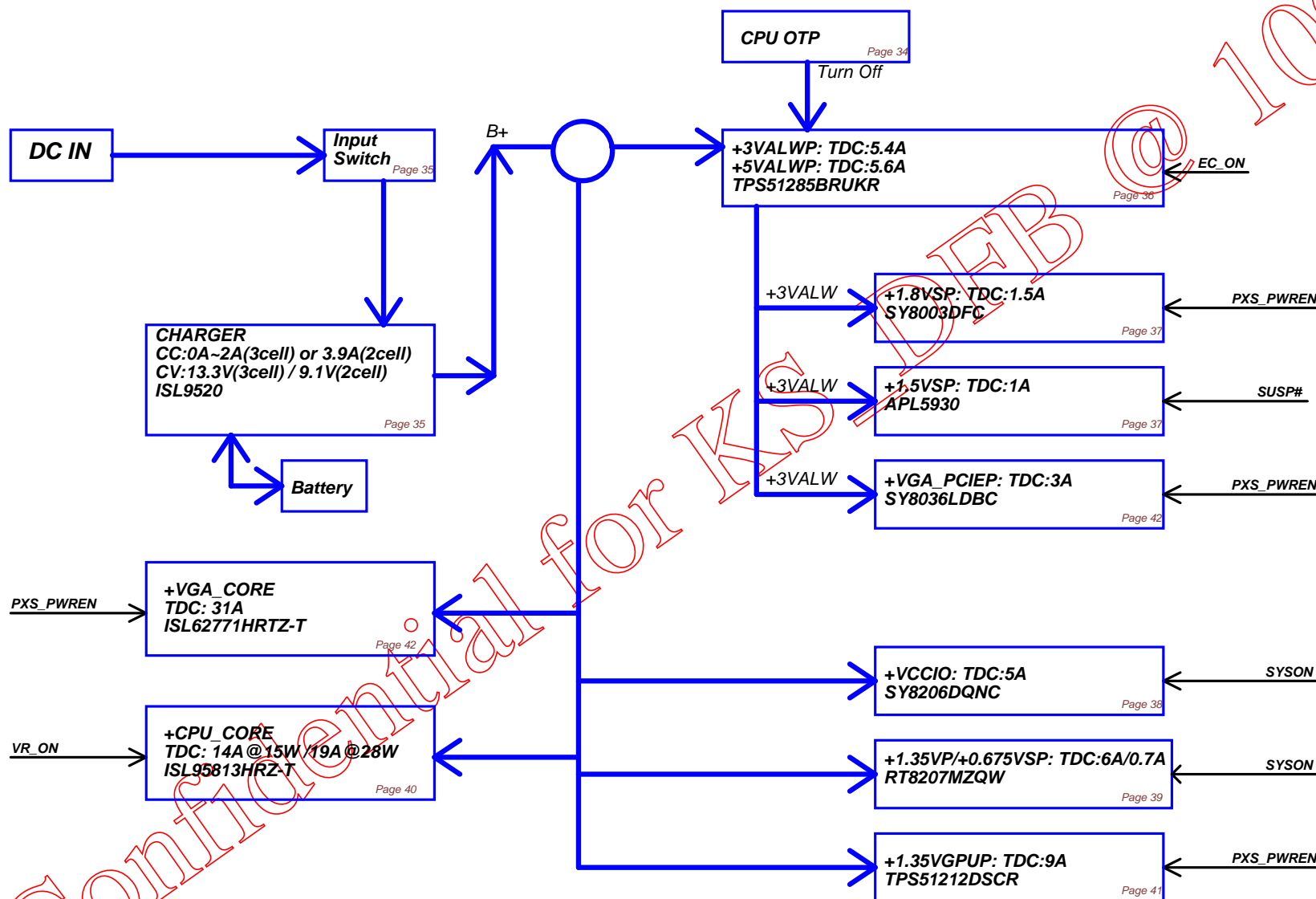






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				Date:	Wednesday, September 10, 2014
				Sheet	43 of 56

# Power block

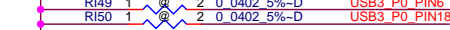
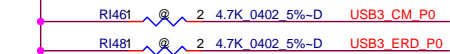
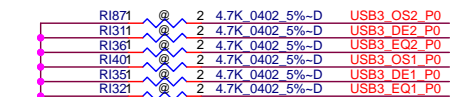
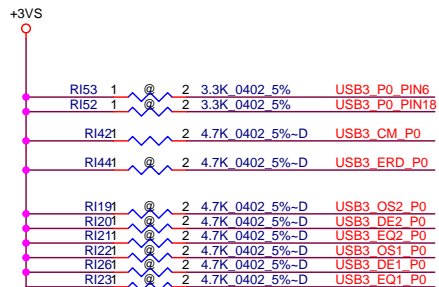


## Version Change List (P. I. R. List)

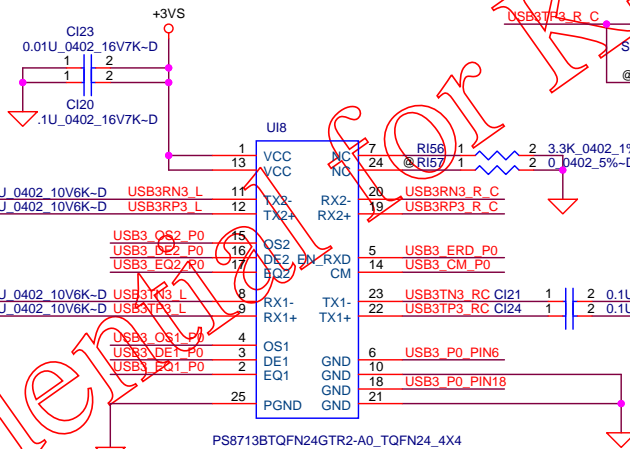
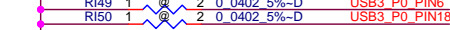
Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.4u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 4.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PR592 from SH00000NM00 to SH00000PQ00 change PR535(15W) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W) from 432 to 261 change PR507(28W) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change Lk	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W) from 169K to 90.9K change PR507(28W) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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		LA-B012P	1.0
		Date:	Wednesday, September 10, 2014 1 Sheet 45 of 56



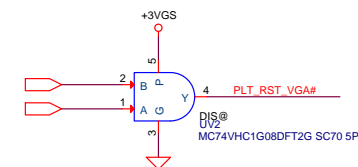
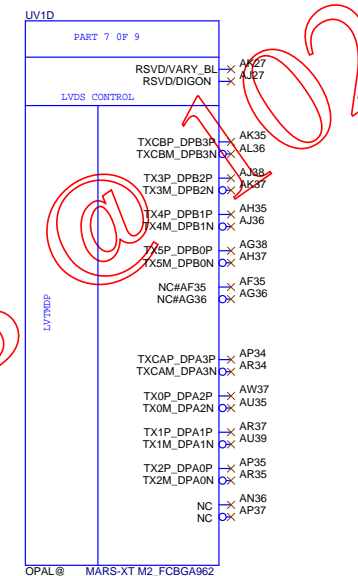
Vendor	PS8713B	TI	Spec	schematic netname	3Vs	GND
1	VDD	VCC	Same			
2	B_EQ0	EQ1	LL: 9.5dB (default) LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_EQ1_P0	R123	@ R132 @
3	DE0	DE1	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE1_P0	R126	@ R135 @
4	EQ1	OS1	LL: 9.5dB LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_OS1_P0	R122	@ R140 @
5	PD#	EN_RXD	it can be left open	USB3_ERD_P0	R144	@ R148 @
6	B_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN6	R153	@ R149 @
7	REXT	NC	4.99K			R156 4.99K
8	B_ina	RX1-	Same			
9	B_ina	RX1+	Same			
10	GND	GND	Same			
11	A_OUTa	TX2-	Same			
12	A_OUTa	TX2+	Same			
13	VDD	VCC	Same			
14	TS1/NC	CM	4.7K ohm resistor for performance adjustment	USB3_CM_P0	R142	@ R146 @
15	A_EQ1	OS2	LL: 9.5 dB (default) LH: 13 dB	USB3_OS2_P0	R119	@ R187 @
16	A_DE0	DE2	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE2_P0	R120	@ R131 @
17	A_EQ0	EQ2	LL: 9.5 dB (default) LH: 13 dB	USB3_EQ2_P0	R121	@ R136 @
18	A_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN18	R152	@ R150 @
19	A_ina	RX2-	Same			
20	A_ina	RX2+	Same			
21	GND	GND	Same			
22	B_OUTa	TX1+	Same			
23	B_OUTa	TX1-	Same			
24	I2C_EN	NC	this pin can be NC or connected to GND	NC		R157 @



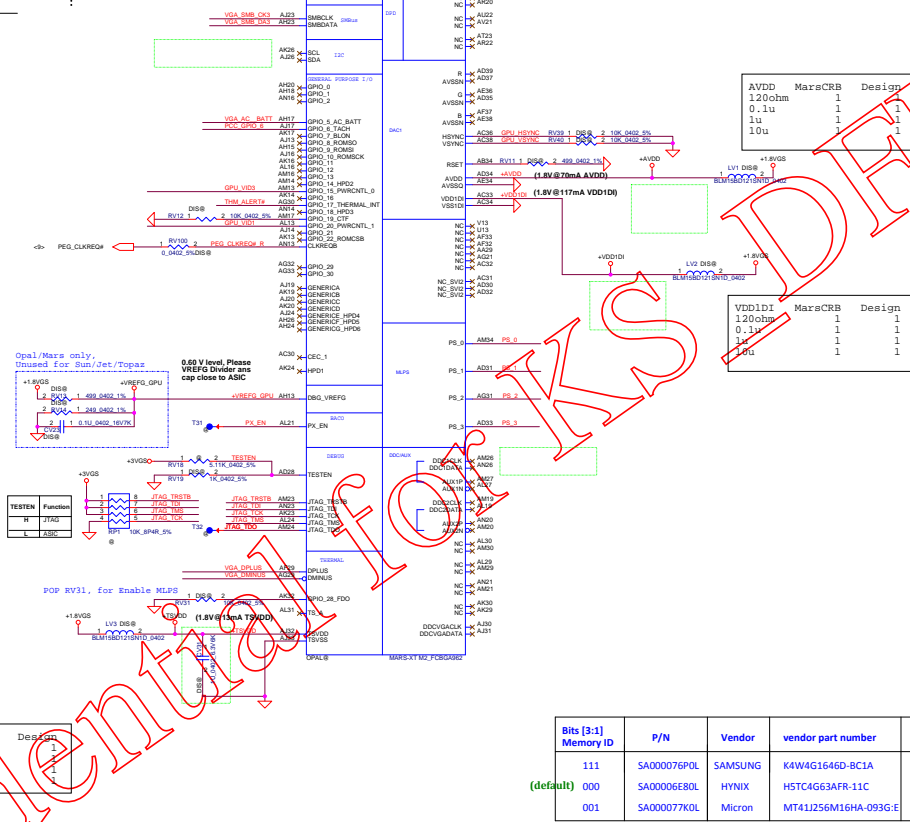
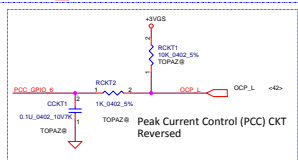
<12> PEG\_CTX\_GRX\_P[3..0] PEG\_CTX\_GRX\_P[3..0]  
<12> PEG\_CTX\_GRX\_N[3..0] PEG\_CTX\_GRX\_N[3..0]



## LVDS Interface



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				Date:	Wednesday, September 10, 2014	Sheet 47 of 56



## MLPS Strap

	Strap[2-1]	Capacitor	R_po	R_pd
PS_05[1]	1 1	001	NC	8.45K 2K
PS_15[1]	1 1	0 0 0	NC	NC
PS_25[1]	1 1	0 0 0	NC	NC
PS_35[1]	1 1	X X X	NC	X X

Mapping to VRAM type please refer to memory table.

+VDDGS

The diagram illustrates the electrical connections for the MLPS Strap configuration. It shows a series of resistors (R1 through R10) connected to the straps of the MLPS Strap. The straps are labeled PS\_05[1], PS\_15[1], PS\_25[1], and PS\_35[1]. The connections are as follows:

- PS\_05[1] is connected to R1 (8.45K) and R2 (2K).
- PS\_15[1] is connected to R3 (8.45K) and R4 (2K).
- PS\_25[1] is connected to R5 (8.45K) and R6 (2K).
- PS\_35[1] is connected to R7 (8.45K) and R8 (2K).

The resistors are connected to the straps of the MLPS Strap, which are labeled PS\_05[1], PS\_15[1], PS\_25[1], and PS\_35[1]. The connections are as follows:

- PS\_05[1] is connected to R1 (8.45K) and R2 (2K).
- PS\_15[1] is connected to R3 (8.45K) and R4 (2K).
- PS\_25[1] is connected to R5 (8.45K) and R6 (2K).
- PS\_35[1] is connected to R7 (8.45K) and R8 (2K).

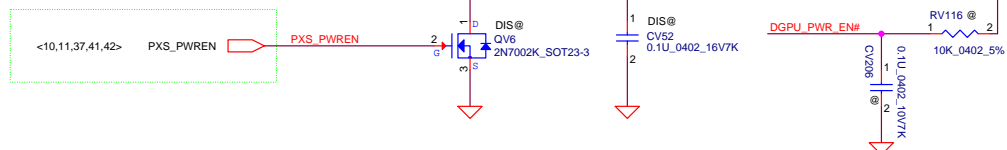
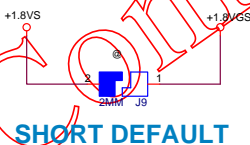
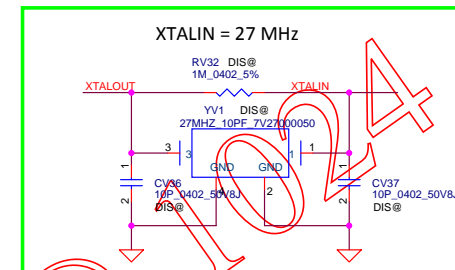
Place CLOSE VGA CHIP

Bits [3:1] Memory ID	P/N	Vendor	vendor part number	Size	RV20	RV27
111	SA000076PDL	SAMSUNG	K4W4G1646D-8C1A	4GB	4.75K	NC
000	SA00006E80L	HYNIX	H5TC4G63AFR-11C	4GB	NC	4.75K
001	SA000077K0L	Micron	MT41J256M16HA-093G:E	4GB	8.45K	2.5K

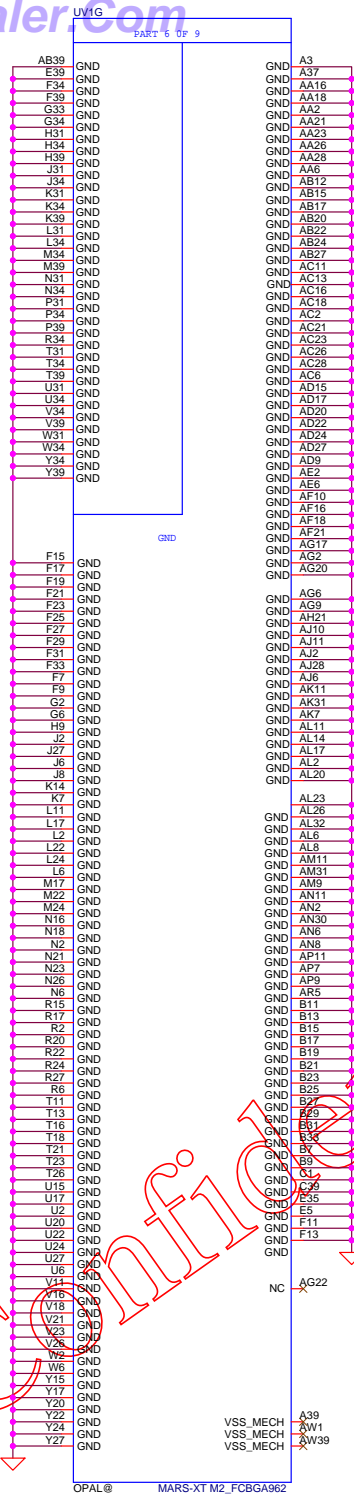
MLPS implementation:

- ★ Place MLPS circuit components as close to ASIC as possible
- ★ Total DC resistance of trace between PS pin and C should be less than 2 ohm
- ★ Total DC resistance of trace between C and ground should be less than 2 ohm
- ★ Trace capacitance should be less than 100pf.
- ★ Resistors should be of  $\pm 1\%$  tolerance

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



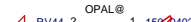
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				Rev.	0.
Date: Wednesday, September 10, 2014				Sheet	49 of 56



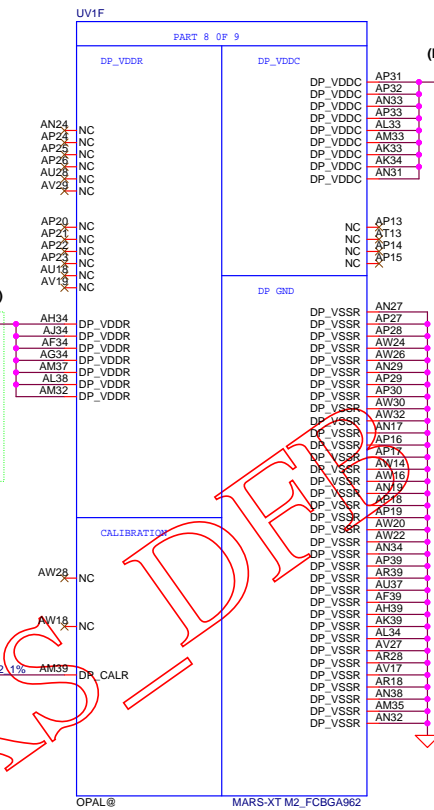
DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1


 +1.8VGS  
 RV43  
 0.0402\_5%  
 (DP\_VDDR:1.8V@237mA/link)  
 +DP\_VDDR

AH34,AJ34,AF34,AG34,AM37,AL38  
For MARS/OPAL only,  
Leave NC on SUN/JET/TOPAZ  
(reference AMD CRB)



RV44  
FOR MARS/OPAL only,  
Leave NC on SUN/JET/TOPIAZ  
(reference AMD CRB)



(DP\_VDDC:0.95V@280mA/link )

DP_VDPC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

FOR MARS/OPAL only,  
Leave NC on SUN/JET/TOPAZ  
(reference AMD CRB)

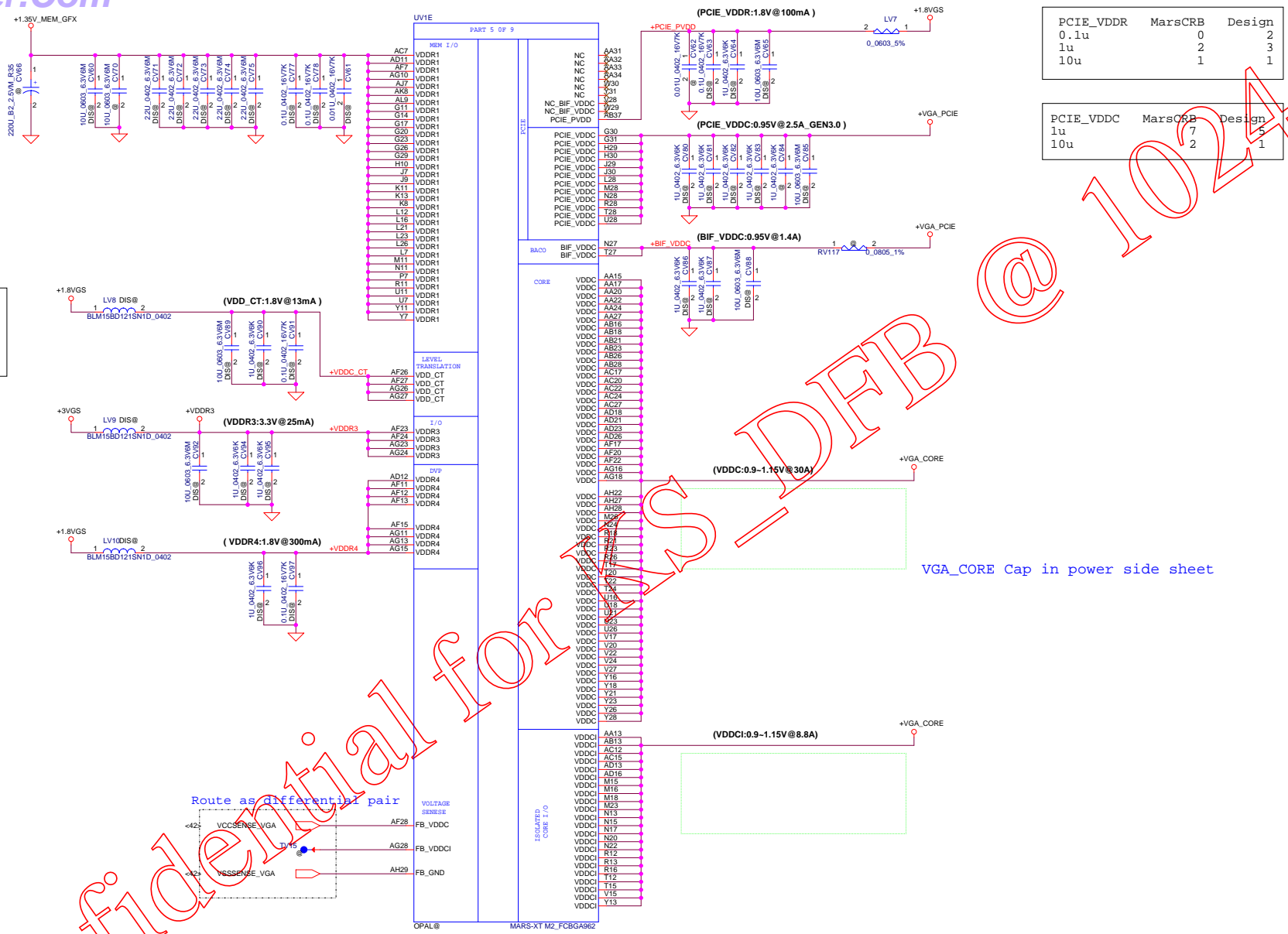
PS. Not include AN32

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

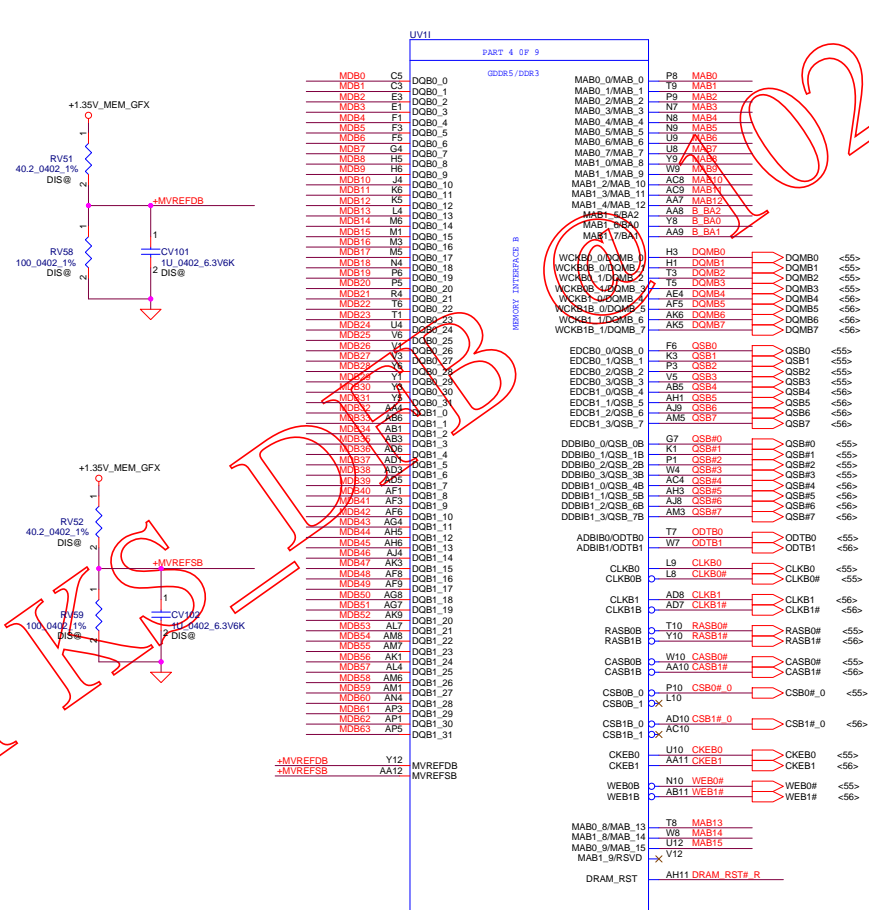
VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



The image shows a detailed PCB layout for the MARS-X1 M2\_FCBGA962 board. The layout is divided into several functional areas:

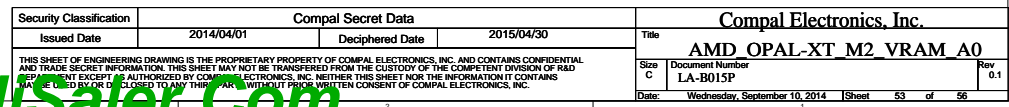
- Power Planes:** The top and bottom layers are primarily copper, with a central area reserved for the processor and its associated components.
- Decoupling Capacitors:** Numerous capacitors are placed across the board to filter noise and stabilize the power supply. These include electrolytic capacitors (e.g., 100µF, 10µF) and ceramic capacitors (e.g., 100nF, 10nF, 1µF).
- Signal Traces:** The layout shows various signal traces, including LVDS signals (LV9, LV10) and differential pairs (VCCSENSE\_VGA, VSSSENSE\_VGA).
- Processor and Core:** The central area contains the processor (MARS-X1 M2\_FCBGA962) and its associated core components, including the OPAL and MARS-X1 M2\_FCBGA962.
- Connectors and I/O:** The layout includes connectors for LVDS signals (LV9, LV10) and other I/O signals (VGA, VGA\_CORE).

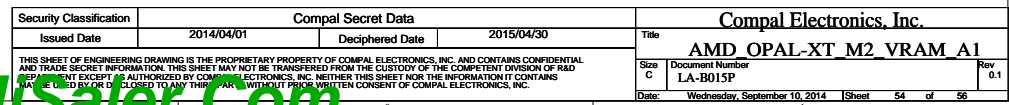
The layout is marked with various labels and dimensions, indicating the precise placement and size of components. A large red watermark "Confidential for AS/DFB" is overlaid on the image, and a large red watermark "AS/DFB" is also visible.

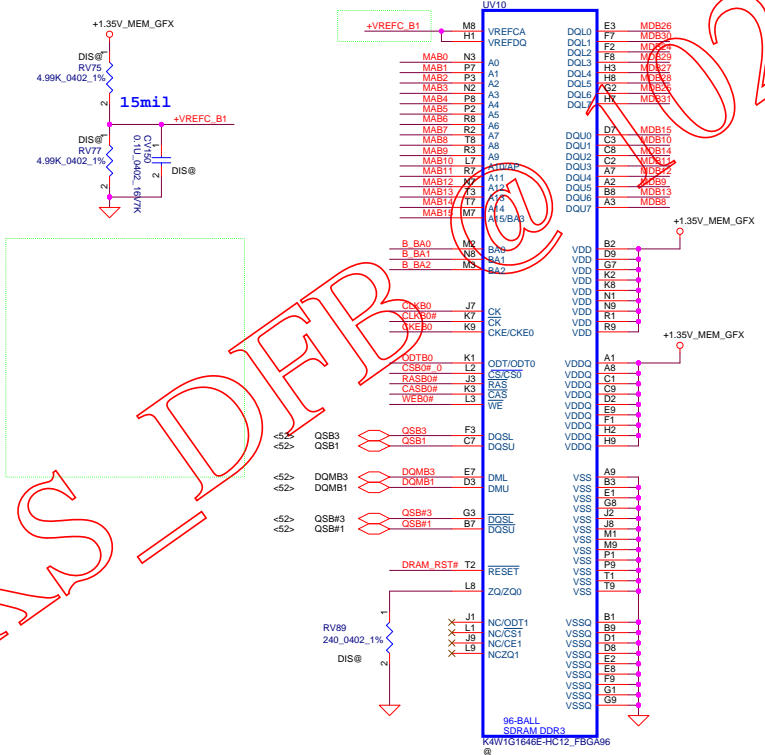


Ball to RV57 < 1"  
CV100 to RV57 < 200 mil  
CV100 to RV53 < 1"

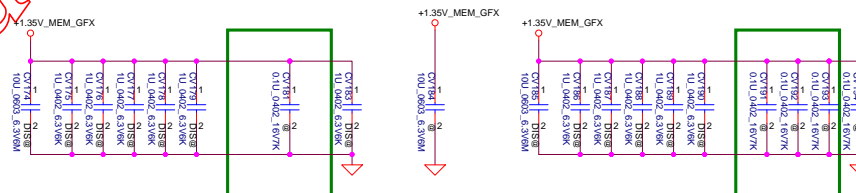
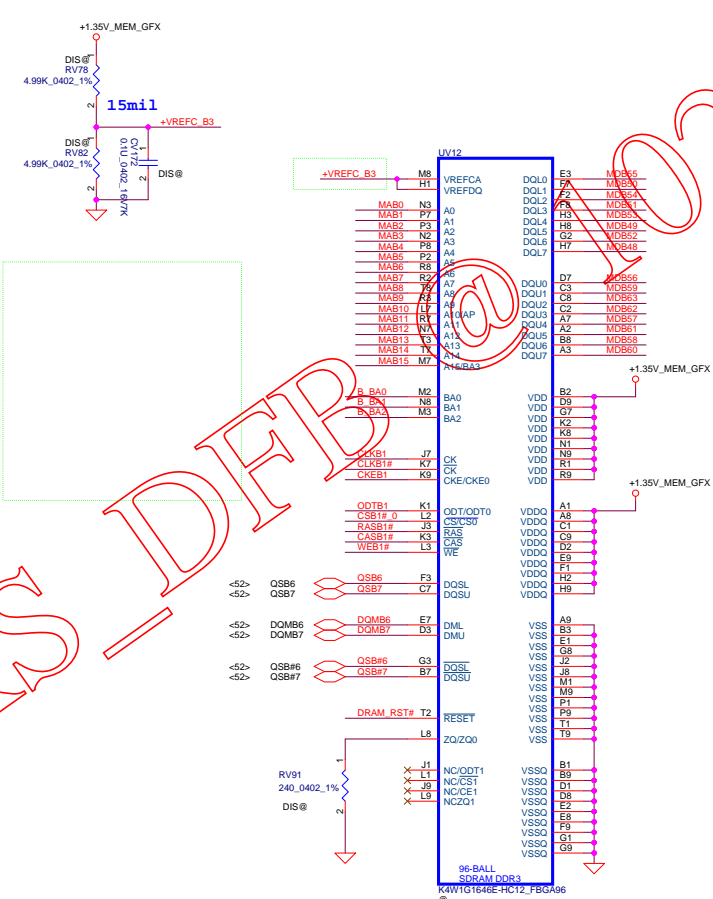
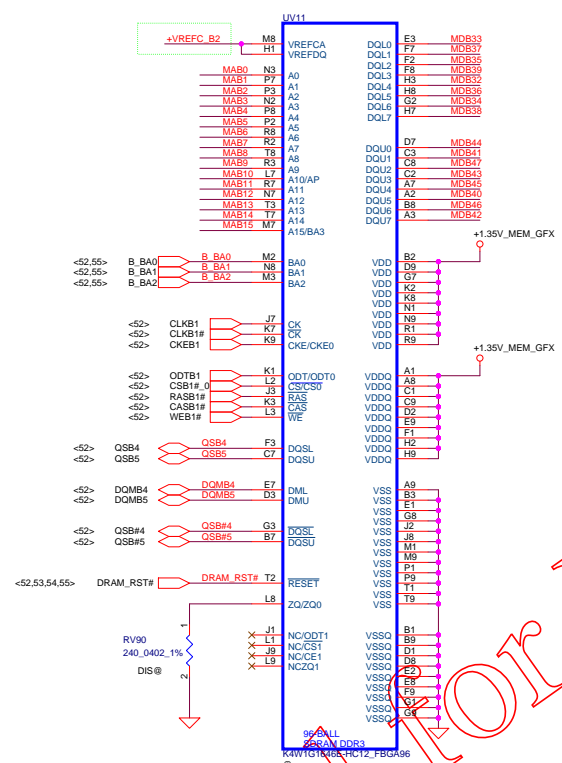
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				Date:	Wednesday, September 10, 2014	Sheet



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				Rev 0.1	
				Date: Wednesday, September 10, 2014	Sheet 56 of 56